Agilent X-Series
Signal Analyzer

This manual provides documentation for the following X-Series Analyzers:

PXA Signal Analyzer N9030A
MXA Signal Analyzer N9020A
EXA Signal Analyzer N9010A

N9073A-1FP W-CDMA Measurement Application & N9073A-2FP HSDPA/HSUPA Measurement Application Measurement Guide

Agilent Technologies

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1 Making W-CDMA with HSDPA/HSUPA Measurements

This chapter begins with instructions common to all measurements, then details all the measurements available by pressing the **Meas** key when the **W-CDMA with HSDPA/HSUPA** mode is selected. For information specific to individual measurements, see the sections at the page numbers below.

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Setting Up and Making a Measurement

Making the Initial Signal Connection

CAUTION Before connecting a signal to the analyzer, make sure the analyzer can safely accept the signal level provided. The signal level limits are marked next to the RF Input connectors on the front panel.

See the Input Key menu for details on selecting input ports and the AMPTD Y Scale menu for details on setting internal attenuation to prevent overloading the analyzer.

Using Analyzer Mode and Measurement Presets

To set your current measurement mode to a known factory default state, press **Mode Preset**. This initializes the analyzer by returning the mode setup and all of the measurement setups in the mode to the factory default parameters.

To preset the parameters that are specific to an active, selected measurement, press **Meas Setup**, **Meas Preset**. This returns all the measurement setup parameters to the factory defaults, but only for the currently selected measurement.

The 3 Steps to Set Up and Make Measurements

All measurements can be set up using the following three steps. The sequence starts at the Mode level, is followed by the Measurement level, then finally, the result displays may be adjusted.

Table 1-1 **The 3 Steps to Set Up and Make a Measurement**

Step	Action	Notes
1. Select and Set Up the Mode	a. Press **Mode** b. Press a mode key, like **Spectrum Analyzer, W-CDMA with HSDPA/HSUPA**, or **GSM/EDGE**. c. Press **Mode Preset**. d. Press **Mode Setup**	All licensed, installed modes available are shown under the **Mode** key. Using **Mode Setup**, make any required adjustments to the mode settings. These settings will apply to all measurements in the mode.
2. Select and Set Up the Measurement	a. Press **Meas.** b. Select the specific measurement to be performed. c. Press **Meas Setup**	The measurement begins as soon as any required trigger conditions are met. The resulting data is shown on the display or is available for export. Use Meas Setup to make any required adjustment to the selected measurement settings. The settings only apply to this measurement.

Table 1-1   The 3 Steps to Set Up and Make a Measurement

Step	Action	Notes
3. Select and Set Up a View of the Results	Press **View/Display**. Select a display format for the current measurement data.	Depending on the mode and measurement selected, other graphical and tabular data presentations may be available. **X-Scale** and **Y-Scale** adjustments may also be made now.

NOTE   A setting may be reset at any time, and will be in effect on the next measurement cycle or view.

Table 1-2   Main Keys and Functions for Making Measurements

Step	Primary Key	Setup Keys	Related Keys
1. Select and set up a mode.	**Mode**	**Mode Setup, FREQ Channel**	**System**
2. Select and set up a measurement.	**Meas**	**Meas Setup**	**Sweep/Control**, **Restart**, **Single, Cont**
3. Select and set up a view of the results.	**View/Display**	**SPAN X Scale, AMPTD Y Scale**	**Peak Search, Quick Save, Save, Recall, File, Print**

2   Channel Power Measurements

This chapter explains how to make a channel power measurement on a W-CDMA mobile station (MS). This test measures the total RF power present in the channel. The results are shown in a graph window and in a text window. If you install the optional HSDPA/HSUPA measurement application license, Code Domain and Modulation Accuracy can measure HSDPA/HSUPA signals as well.

Setting Up and Making a Measurement

Configuring the Measurement System

The MS under test must be set to transmit the RF power remotely through the system controller. This transmitting signal is connected to the RF input port of the instrument. Connect the equipment as shown.

Figure 2-1   **Channel Power Measurement System**

1. Using the appropriate cables, adapters, and circulator, connect the output signal from the MS to the RF input port of the analyzer.

2. Connect the base transceiver station simulator or signal generator to the MS through the circulator to initiate a link constructed with the sync and pilot channels, if required.

3. Connect a BNC cable between the 10 MHz OUT port of the signal generator and the EXT REF IN port of the analyzer.

4. Connect the system controller to the MS through the serial bus cable to control the MS operation.

Setting the MS (Example)

From the transceiver station simulator or the system controller, or both, perform all of the call acquisition functions required for the MS to transmit the RF power as follows:

Frequency: 1920 MHz (Channel Number: $5 \times 1920 = 9600$)

Output Power: –20 dBm (at analyzer input)

Measurement Procedure

Step 1. Press **Mode**, **W-CDMA with HSDPA/HSUPA** to enable the W-CDMA measurements.

Step 2. Press **Mode Preset** to preset the Mode.

Step 3. Press **Mode Setup**, **Radio**, **Device** to toggle the device to **MS**.

Step 4. Press **FREQ Channel**, **1920**, **MHz** to set the center frequency to 1.920 GHz.

Step 5. Press **Meas**, **Channel Power** to initiate the channel power measurement.

The Channel Power measurement result should look similar to Figure 2-2. The graph window and the text window show the absolute power and its mean power spectral density values over 5 MHz.

Figure 2-2 **Channel Power Measurement Result**
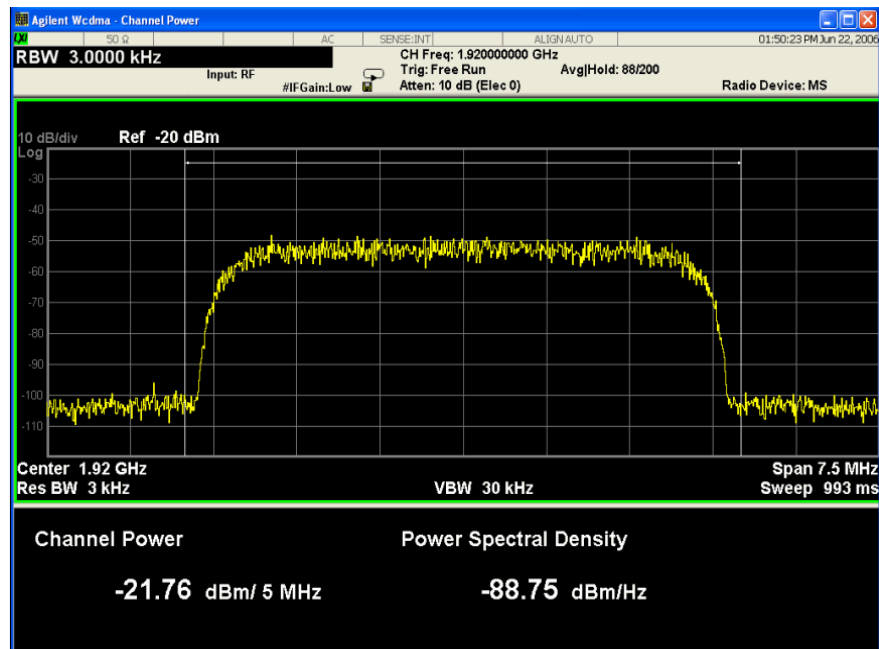
Step 6. Press **Meas Setup** to see the keys that are available to change measurement parameters from their default condition.

If you have a problem, and get an error message, see the "*Error Messages Guide*".

3 ACP Measurements

This chapter explains how to make the adjacent channel leakage power ratio (ACLR or ACPR) measurement on a W-CDMA mobile station (MS). ACPR is a measurement of the amount of interference, or power, in an adjacent frequency channel. The results are shown as a bar graph or as spectrum data, with measurement data at specified offsets.

Setting Up and Making a Measurement

Configuring the Measurement System

The MS under test must be set to transmit the RF power remotely through the system controller. This transmitting signal is connected to the RF input port of the instrument. Connect the equipment as shown.

Figure 3-1   **Adjacent Channel Power Ratio Measurement System**

1. Using the appropriate cables, adapters, and circulator, connect the output signal from the MS to the RF input port of the analyzer.

2. Connect the base transceiver station simulator or signal generator to the MS through the circulator to initiate a link constructed with the sync and pilot channels, if required.

3. Connect a BNC cable between the 10 MHz OUT port of the signal generator and the EXT REF IN port of the analyzer.

4. Connect the system controller to the MS through the serial bus cable to control the MS operation.

Setting the MS (Example)

From the transceiver station simulator or the system controller, or both, perform all of the call acquisition functions required for the MS to transmit the RF power as follows:

Frequency: 1920 MHz (Channel Number: $5 \times 1920 = 9600$)

Physical Channels: DPCCH with 4 DPDCH

Scramble Code: 0

Output Power: –20 dBm (at analyzer input)

Measurement Procedure

Step 1. Press **Mode**, **W-CDMA with HSDPA/HSUPA** to enable the W-CDMA measurements.

Step 2. Press **Mode Preset** to preset the mode.

Step 3. Press **Mode Setup**, **Radio**, **Device** to toggle the device to **MS**.

Step 4. Press **FREQ Channel**, **1920**, **MHz** to set the center frequency to 1.920 GHz.

Step 5. Press **Meas**, **ACP** to initiate the adjacent channel leakage power ratio measurement.

Step 6. Press **View/Display**, and toggle the **Bar Graph** key to **Off** to see the spectrum trace graph.

Figure 3-2   **Measurement Result - Spectrum Trace Graph View**
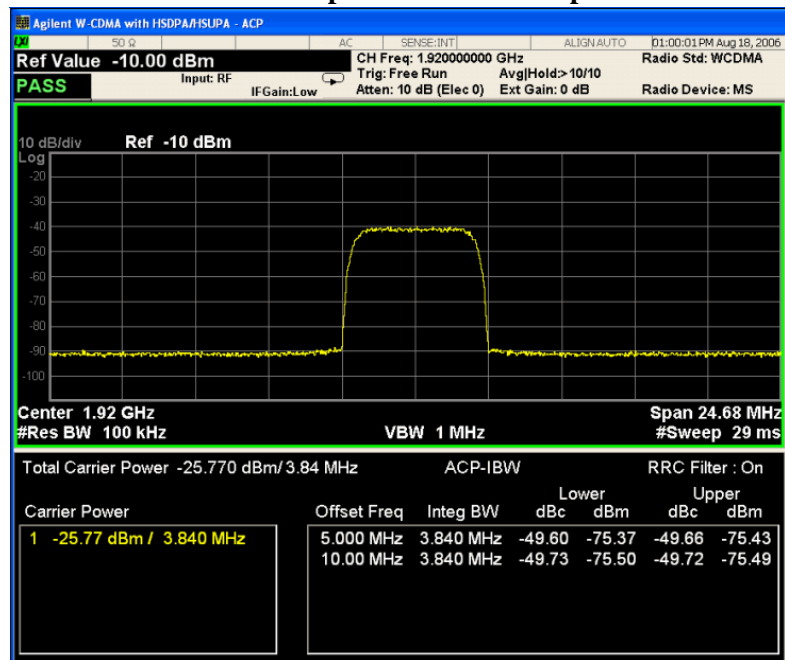
The spectrum graph measurement result should look similar to Figure 3-2. The graph (referenced to the total power) and a text window are displayed. The text window shows the absolute total power reference, while the lower and upper offset channel power levels are displayed in both absolute and relative readings.

Step 7. Press **View/Display**, and toggle the **Bar Graph** key to **On** to see the bar graph with the spectrum trace graph overlay. The corresponding measured data is also shown in the text window. See Figure 3-3.

Figure 3-3   **Measurement Result - Bar Graph View (Default)**
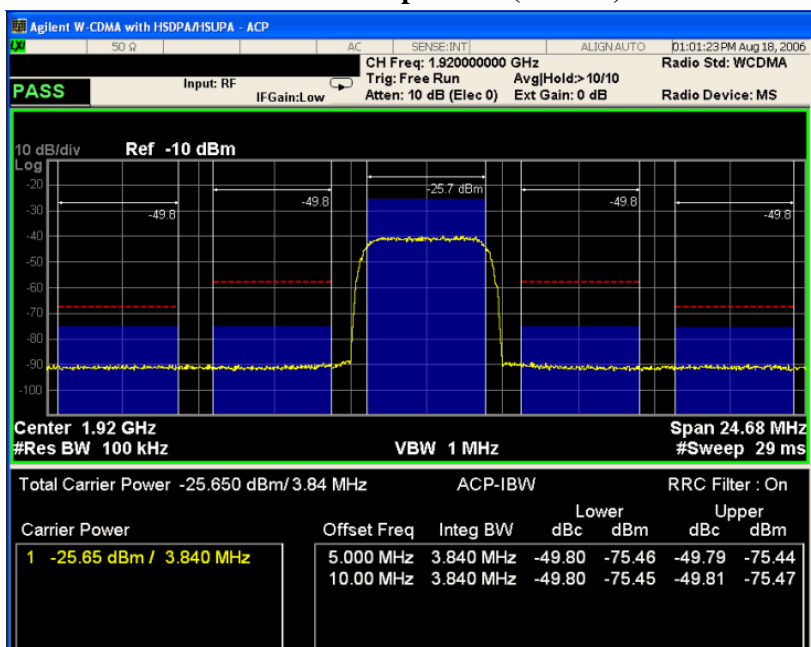
Step 8. Press **Meas Setup**, **Meas Method**, and select **Fast**. The measurement result display is shown in Figure 3-4.

Figure 3-4   **Fast Measurement Result - Bar Graph View**
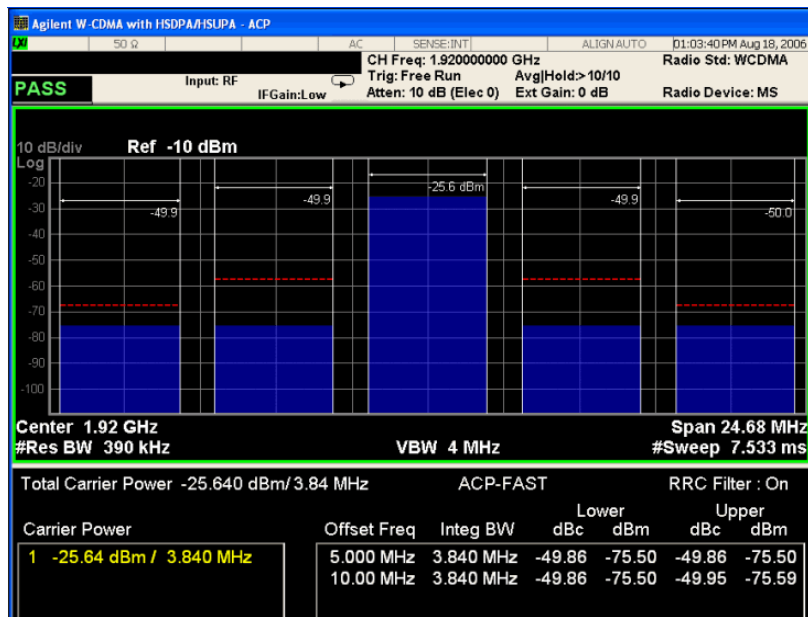
Step 9. Press **Meas Setup** to see the keys that are available to change the measurement parameters from the default condition.

If you have a problem, and get an error message, see the "*Error Messages Guide*".

4   Spectrum Emission Mask Measurements

This chapter explains how to make the spectrum emission mask (SEM) measurement on a W-CDMA mobile station (MS). SEM compares the total power level within the defined carrier bandwidth and the given offset channels on both sides of the carrier frequency, to levels allowed by the standard. Results of the measurement of each offset segment can be viewed separately.

Setting Up and Making a Measurement

Configuring the Measurement System

The MS under test must be set to transmit the RF power remotely through the system controller. This transmitting signal is connected to the RF input port of the instrument. Connect the equipment as shown.

Figure 4-1   **Spectrum Emission Mask Measurement System**

1. Using the appropriate cables, adapters, and circulator, connect the output signal from the MS to the RF input port of the analyzer.

2. Connect the base transceiver station simulator or signal generator to the MS through the circulator to initiate a link constructed with the sync and pilot channels, if required.

3. Connect a BNC cable between the 10 MHz OUT port of the signal generator and the EXT REF IN port of the analyzer.

4. Connect the system controller to the MS through the serial bus cable to control the MS operation.

Setting the MS (Example)

From the base transceiver station simulator or the system controller, or both, perform all of the call acquisition functions required for the MS to transmit the RF power as follows:

Frequency: 1920 MHz (Channel Number: $5 \times 1,920 = 9,600$)

Output Power: 0 dBm (at analyzer input)

Measurement Procedure

Step 1. Press **Mode**, **W-CDMA with HSDPA/HSUPA** to enable the W-CDMA measurements.

Step 2. Press **Mode Preset** to preset the mode.

Step 3. Press **Mode Setup**, **Radio**, **Device** to toggle the device to **MS**.

Step 4. Press **FREQ Channel**, **1920**, **MHz** to set the center frequency to 1.920 GHz.

Step 5. Press **Meas**, **Spectrum Emission Mask** to initiate the spectrum emission mask measurement.

Figure 4-2   **Spectrum Emission Mask Measurement Result**

Agilent W-CDMA with HSDPA/HSUPA - Spectrum Emission Mask

50 Ω — AC — SENSE:INT — ALIGN AUTO — 01:27:21 PM Aug 18, 2006
Y Reference Value 0.00 dBm
CH Freq: 1.920000000 GHz — Radio Std: WCDMA
PASS — Input: RF — Trig: Free Run
IFGain:Low — Atten: 10 dB (Elec 0)   Ext Gain: 0 dB — Radio Device: MS

10 dB/div   Ref 0 dBm
Log

Center 1.92 GHz — Span 24 MHz

Total Pwr Ref   -5.49 dBm /   3.84 MHz

				Lower		<- Peak ->	Upper	
Start Freq	Stop Freq	Integ BW	dBm	ΔLim(dB)	Freq (Hz)	dBm	ΔLim(dB)	Freq (Hz)
2.515 MHz	3.485 MHz	30.00 kHz	-74.04	(-20.85)	-3.446 M	-70.70	(-21.59)	3.175 M
4.000 MHz	7.500 MHz	1.000 MHz	-55.64	(-15.84)	-4.315 M	-55.35	(-15.72)	4.140 M
7.500 MHz	8.500 MHz	1.000 MHz	-70.34	(-17.90)	-8.445 M	-70.50	(-18.06)	8.445 M
8.500 MHz	12.00 MHz	1.000 MHz	-68.13	(-15.14)	-10.36 M	-68.33	(-15.34)	9.970 M
12.50 MHz	15.00 MHz	1.000 MHz	---	(---)	---	---	(---)	---
15.00 MHz	18.00 MHz	1.000 MHz	---	(---)	---	---	(---)	---

The Spectrum Emission Mask measurement result should look similar to Figure 4-2. The text window shows the reference total power and the absolute peak power levels which correspond to the frequency bands on both sides of the reference channel.

If you have a problem, and get an error message, see the "*Error Messages Guide*".

Troubleshooting Hints

This spectrum emission mask measurement can reveal degraded or defective parts in the transmitter section of the unit under test (UUT). The following examples are those areas to be checked further.

- Faulty DC power supply control of the transmitter power amplifier.

- RF power controller of the pre-power amplifier stage.

- I/Q control of the baseband stage.

- Some degradation in the gain and output power level of the amplifier due to the degraded gain control or increased distortion, or both.

- Some degradation of the amplifier linearity or other performance characteristics.

Power amplifiers are one of the final stage elements of a base or mobile transmitter and are a critical part of meeting the important power and spectral efficiency specifications. Since spectrum emission mask measures the spectral response of the amplifier to a complex wideband signal, it is a key measurement linking amplifier linearity and other performance characteristics to the stringent system specifications.

5   Spurious Emissions Measurement

This section explains how to make the spurious emission measurement on a W-CDMA mobile station (MS). This measurement identifies and determines the power level of spurious emissions in certain frequency bands.
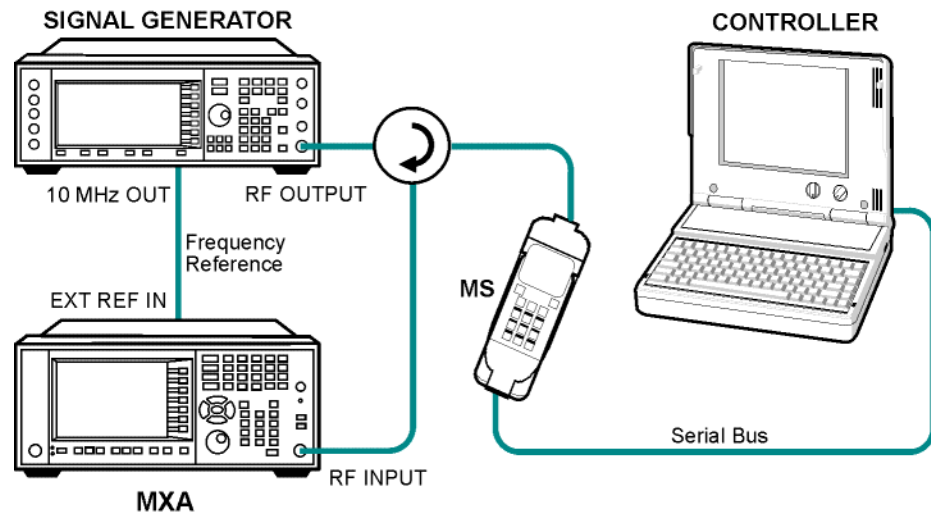
Setting Up and Making a Measurement

Configuring the Measurement System

The MS under test must be set to transmit the RF power remotely through the system controller. This transmitting signal is connected to the RF input port of the instrument. Connect the equipment as shown.

Figure 5-1   **Mobile Station Equipment Measurement System Setup**
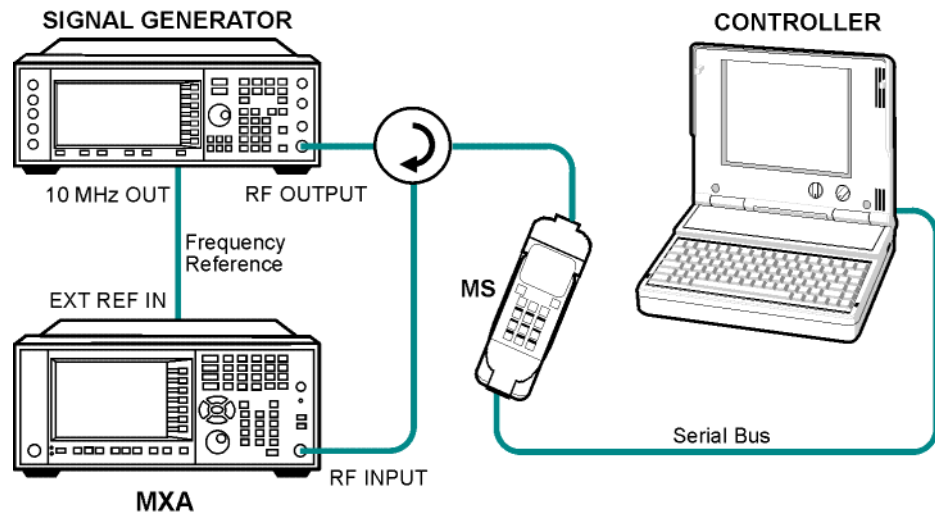
1. Using the appropriate cables, adapters, and circulator, connect the output signal from the MS to the RF input port of the analyzer.

2. Connect the base transceiver station simulator or signal generator to the MS through the circulator to initiate a link constructed with the sync and pilot channels, if required.

3. Connect a BNC cable between the 10 MHz OUT port of the signal generator and the EXT REF IN port of the analyzer.

4. Connect the system controller to the MS through the serial bus cable to control the MS operation.

Setting up the MS (Example)

From the system controller, perform all of the call acquisition functions required for the MS to transmit the RF power as required.
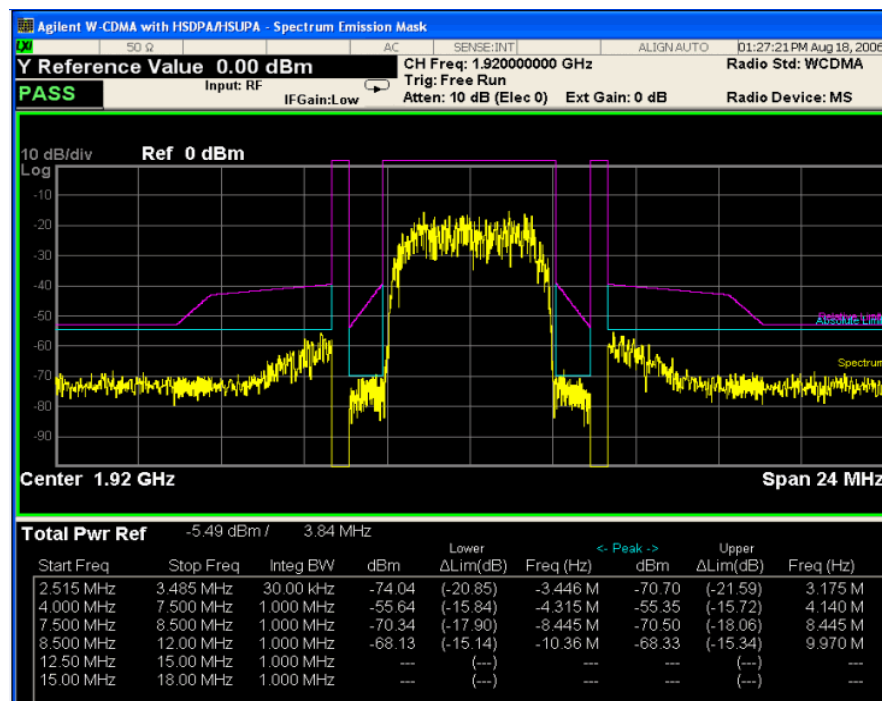
Measurement Procedure

Step 1. Press **Mode**, **W-CDMA with HSDPA/HSUPA** to enable the W-CDMA measurements.

Step 2. Press **Mode Preset** to preset the mode.

Step 3. Press **Input/Output**, **RF Input**, **RF Coupling** to toggle the RF Coupling to **DC**.

Step 4. Press **Mode Setup**, **Radio**, **Device** to toggle the device to **MS**.

Step 5. Press **FREQ Channel**, enter a numerical frequency using the front-panel keypad, and select a units key, such as **MHz**.

Step 6. Press **Meas**, **Spurious Emission** to initiate the spurious emission measurement.

Depending on the current settings, the instrument will begin making the selected measurements. The resulting data is shown on the display or available for export.

If you want to change the measurement parameters from their default condition for a customized measurement, press **Meas Setup** to see the parameter keys that are available.

Measurement Results

The Spurious Emissions measurement results should look similar to Figure 5-2. The spectrum window and the text window show the spurs that are within the current value of the Marker Peak Excursion setting of the absolute limit. Any spur that has failed the absolute limit will have an 'F' beside it.

Figure 5-2   **Spurious Emissions Measurement**
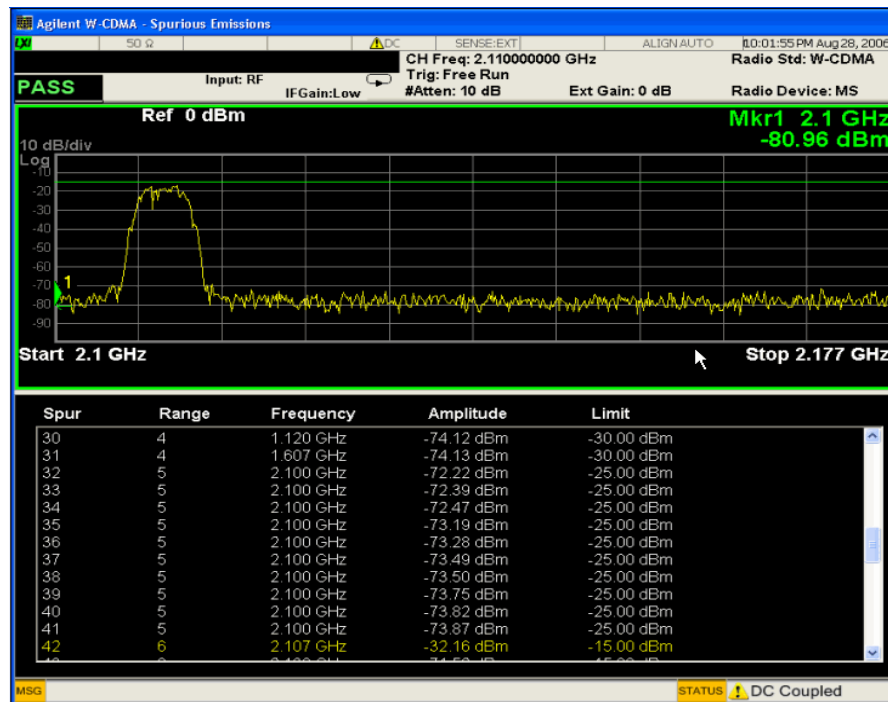
If you have a problem, and get an error message, see the "*Error Messages Guide*".

6 Occupied Bandwidth Measurements

This chapter explains how to make the occupied bandwidth measurement on a W-CDMA mobile station (MS). The instrument measures power across the band, and then calculates its 99.0% power bandwidth.

Setting Up and Making a Measurement

Configuring the Measurement System

The MS under test must be set to transmit the RF power remotely through the system controller. This transmitting signal is connected to the RF input port of the instrument. Connect the equipment as shown.

Figure 6-1   **Occupied Bandwidth Measurement System**

1. Using the appropriate cables, adapters, and circulator, connect the output signal of the MS to the RF input of the analyzer.

2. Connect the base transceiver station simulator or signal generator to the MS through the circulator to initiate a link constructed with the sync and pilot channels, if required.

3. Connect a BNC cable between the 10 MHz OUT port of the signal generator and the EXT REF IN port of the analyzer.

4. Connect the system controller to the MS through the serial bus cable to control the MS operation.

Setting the MS (Example)

From the base transceiver station simulator or the system controller, or both, perform all of the call acquisition functions required for the MS to transmit the RF power as follows:

Frequency: 1920 MHz (Channel Number: $5 \times 1,920 = 9,600$)

Output Power: –20 dBm (or other power level for the MS)

Measurement Procedure

Step 1. Press **Mode**, **W-CDMA with HSDPA/HSUPA** to enable the W-CDMA measurements.

Step 2. Press **Mode Preset** to preset the mode.

Step 3. Press **Mode Setup**, **Radio**, **Device** to toggle the device to **MS**.

Step 4. Press **FREQ Channel**, **1920**, **MHz** to set the center frequency to 1.920 GHz.

Step 5. Press **Meas**, **Occupied BW** to initiate the occupied bandwidth measurement.

The Occupied BW measurement result should look similar to the Figure 6-2.

Figure 6-2   **Occupied Bandwidth Measurement Result**
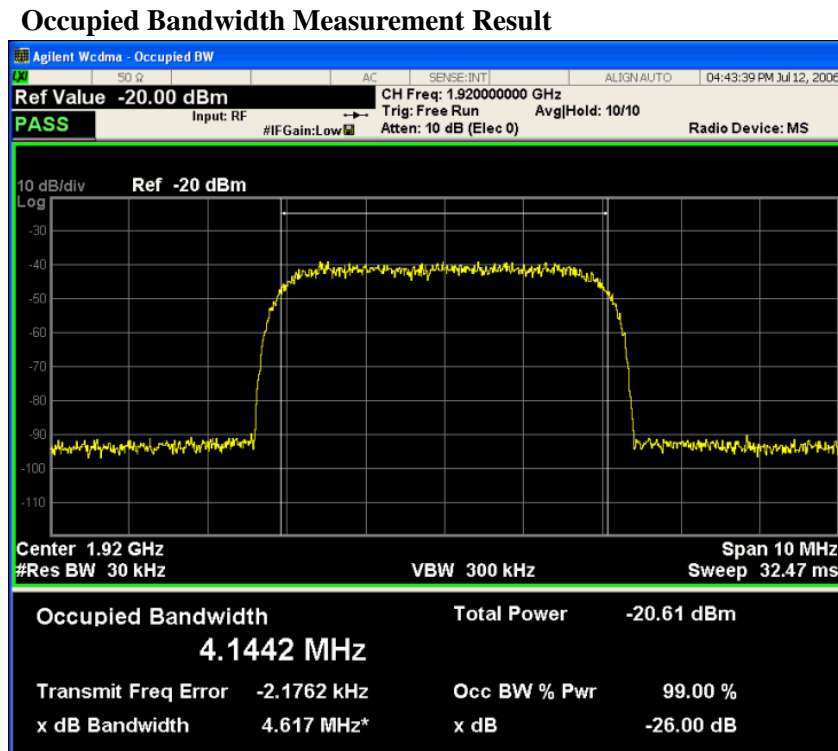
If you have a problem, and get an error message, see the "*Error Messages Guide*".

Troubleshooting Hints

Any distortion such as harmonics or intermodulation, for example, produces undesirable power outside the specified bandwidth.

Shoulders on either side of the spectrum shape indicate spectral regrowth and intermodulation. Rounding or sloping of the top shape can indicate filter shape problems.

7   Power Statistics CCDF Measurements

This section explains how to make the Power Statistics Complementary Cumulative Distribution Function (Power Stat CCDF) measurement on a W-CDMA mobile station (MS). Power Stat CCDF curves characterize the higher level power statistics of a digitally modulated signal.
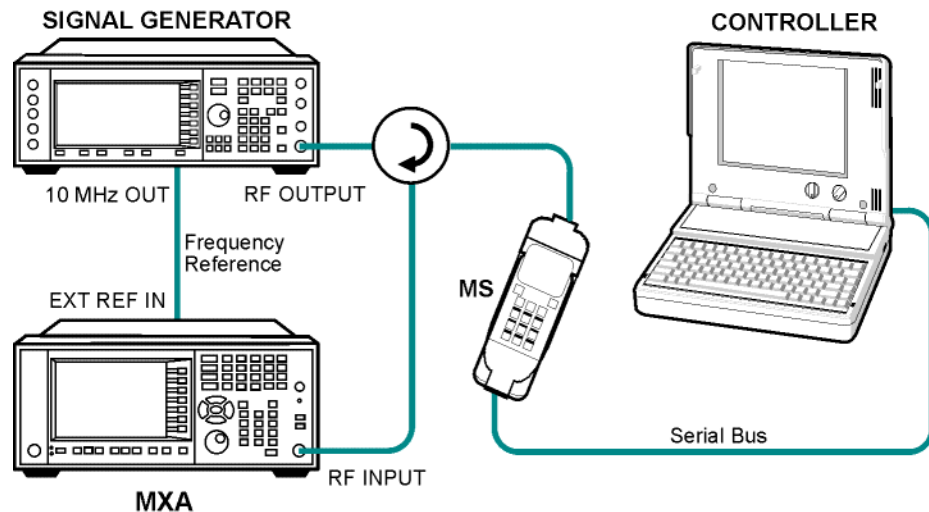
Setting Up and Making a Measurement

Configuring the Measurement System

The mobile station (MS) under test must be set to transmit the RF power remotely through the system controller. This transmitting signal is connected to the RF input port of the instrument. Connect the equipment as shown.

Figure 7-1   **Power Statistics (CCDF) Measurement System**

1. Using the appropriate cables, adapters, and circulator, connect the output signal of the MS to the RF input of the analyzer.

2. Connect the base transceiver station simulator or signal generator to the MS through the circulator to initiate a link constructed with the sync and pilot channels, if required.

3. Connect a BNC cable between the 10 MHz OUT port of the signal generator and the EXT REF IN port of the analyzer.

4. Connect the system controller to the MS through the serial bus cable to control the MS operation.

Setting the MS (Example)

From the base transceiver station simulator or the system controller, or both, perform all of the call acquisition functions required for the MS to transmit the RF power as follows:

Frequency: 1920 MHz (Channel Number: $5 \times 1,920 = 9,600$)

Physical Channels: DPCCH with one or more DPDCH

Output Power: –20 dBm (at analyzer input)

Measurement Procedure

Step 1. Press **Mode**, **W-CDMA with HSDPA/HSUPA** to enable the W-CDMA measurements.

Step 2. Press **Mode Preset** to preset the mode.

Step 3. Press **Mode Setup**, **Radio**, **Device** to toggle the device to **MS**.

Step 4. Press **FREQ Channel**, **1920**, **MHz** to set the center frequency to 1.920 GHz.

Step 5. Press **Meas**, **Power Stat CCDF** to initiate the power statistics CCDF measurement.

The CCDF measurement result should look similar to Figure 7-2.

Figure 7-2   **Power Statistics CCDF Result**
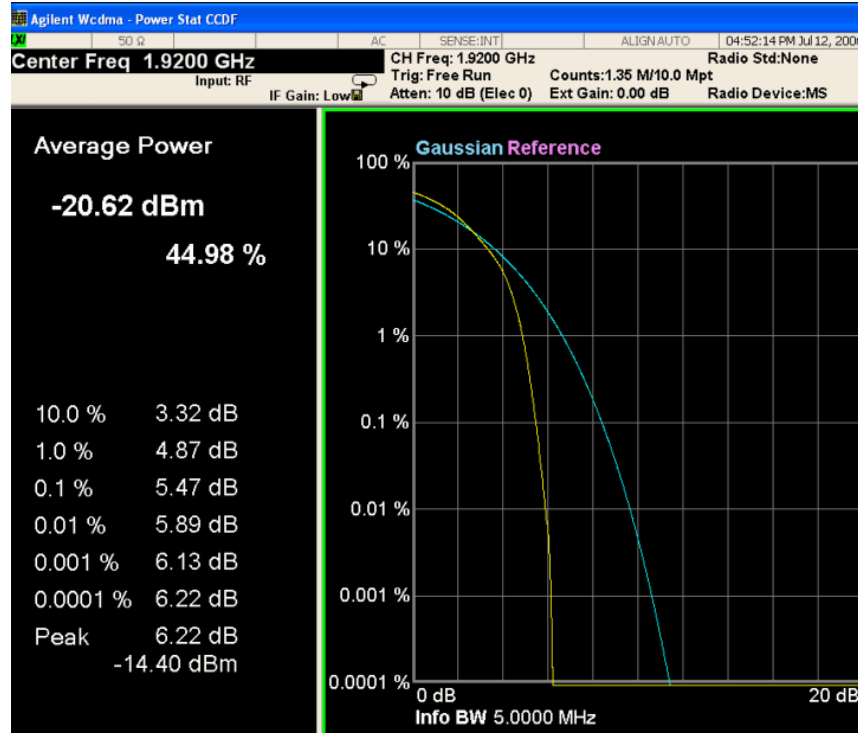
If you have a problem, and get an error message, see the "*Error Messages Guide*".

Troubleshooting Hints

The power statistics CCDF measurement can contribute in setting the signal power specifications for design criteria for systems, amplifiers, and other components. For example, it can help determine the optimum operating point to adjust each code timing for appropriate peak or average power ratio, or both, throughout the wide channel bandwidth of the transmitter for a W-CDMA system.

8   Code Domain Measurements

This chapter explains how to make a code domain measurement on a W-CDMA mobile station (MS) and a base transceiver station (BTS). This is the measurement of power levels of the spread code channels across composite RF channels. The code power may be measured relative to the total power within the 3.840 MHz channel bandwidth, or absolutely, in units of power. Code Domain measurement examples using a W-CDMA uplink (UL) signal and a HSDPA downlink (DL) signal are shown in this section.

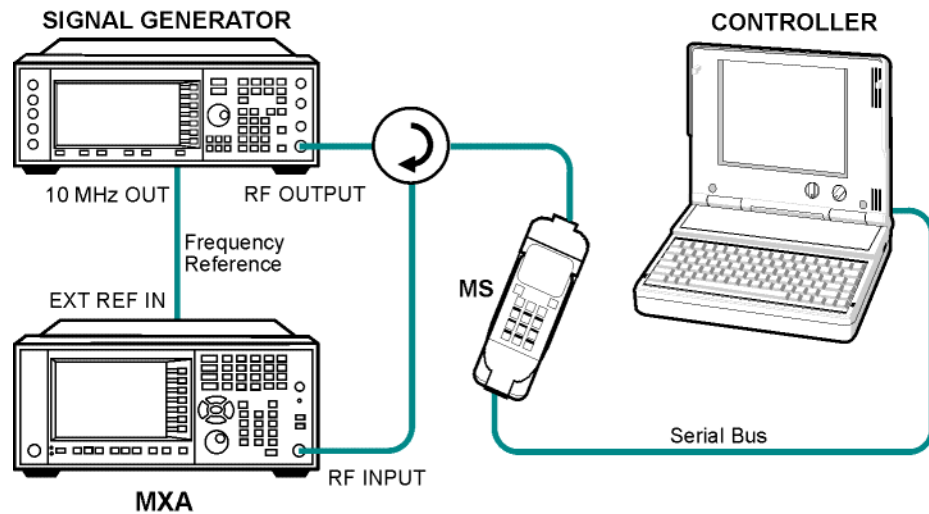## Setting Up and Making a Measurement

Configuring the Measurement System

The MS under test must be set to transmit the RF power remotely through the system controller. This transmitting signal is connected to the RF input port of the instrument. Connect the equipment as shown.

Figure 8-1   **Code Domain Power Measurement System**
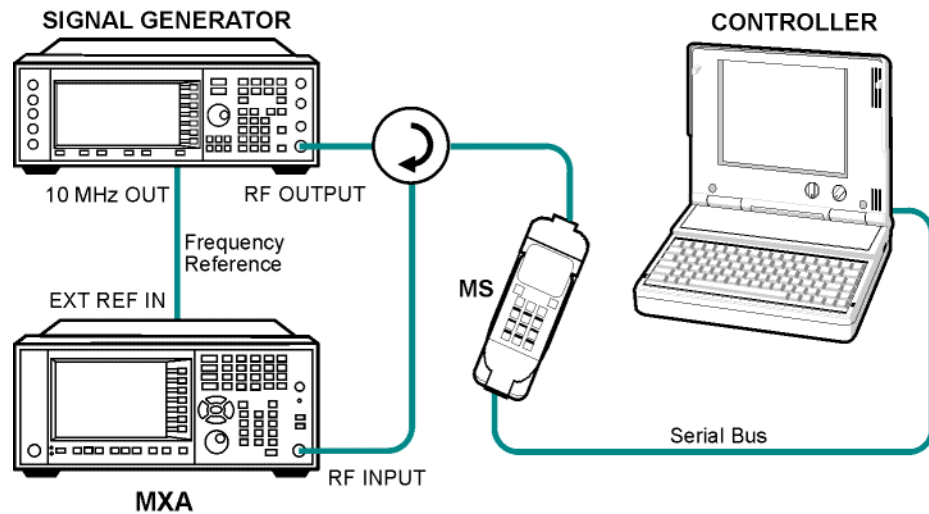
1. Using the appropriate cables, adapters, and circulator, connect the output signal of the MS to the RF input of the instrument.

2. Connect the base transceiver station simulator or signal generator to the MS through the circulator to initiate a link constructed with the sync and pilot channels, if required.

3. Connect a BNC cable between the 10 MHz OUT port of the signal generator and the EXT REF IN port of the instrument.

4. Connect the system controller to the MS through the serial bus cable to control the MS operation.

W-CDMA UL Measurement Example (Normal Mode)

Setting the MS (Example)

From the mobile station simulator or the system controller, or both, perform all of the call acquisition functions required for the MS to transmit the RF power as follows:

Frequency: 1,920 MHz (Channel Number: $5 \times 1,920 = 9,600$)

Physical Channels: DPCCH with 4 DPDCH

Scramble Code: 0

Output Power: –20 dBm (at analyzer input)

Measurement Procedure

Step 1. Press **Mode**, **W-CDMA with HSDPA/HSUPA** to enable the W-CDMA measurements.

Step 2. Press **Mode Preset** to preset the mode.

Step 3. Press **Mode Setup**, **Radio**, **Device** to toggle the device to **MS**.

Step 4. Press **FREQ Channel**, **1920**, **MHz** to set the center frequency to 1.920 GHz.

Step 5. Press **Meas**, **Code Domain** to initiate the code domain measurement. The measurement result should look similar to Figure 8-2. The graph window is displayed with a text window below it. The text window shows the total power level along with the relative power levels of the various channels.

Figure 8-2   **Code Domain Measurement Result - Power Graph & Metrics (Default) View**
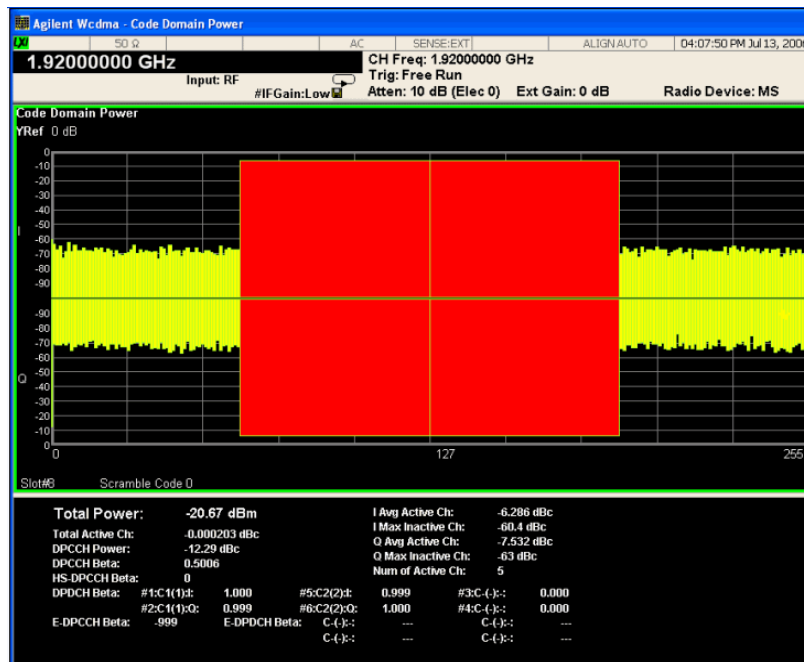
Step 6. Press **Peak Search** to put a marker on the highest power channel. See Figure 8-3. The I branch marker #1 measurement data shows C2(2), which indicates the code channel number 2 with SF 2^2 = 4. It also indicates the channel data rate at 960 ksps, and provides the power measurement of –6.28 dB in the channel relative to the total code power of the signal. The summary data shows active channels to be C1, C2, C5, C6. The Code Domain Power (CDP) and Code Domain Error (CDE) of the channel can be checked with the marker. For correct beta calculation, **DPCH/E-DPCH Config** should be selected correctly under **Meas Setup**.

Figure 8-3 **Code Domain Measurement Result - Power Graph & Metrics View - Uplink (MS) DPCCH, and 4 DPDCH w/ Peak Marker**
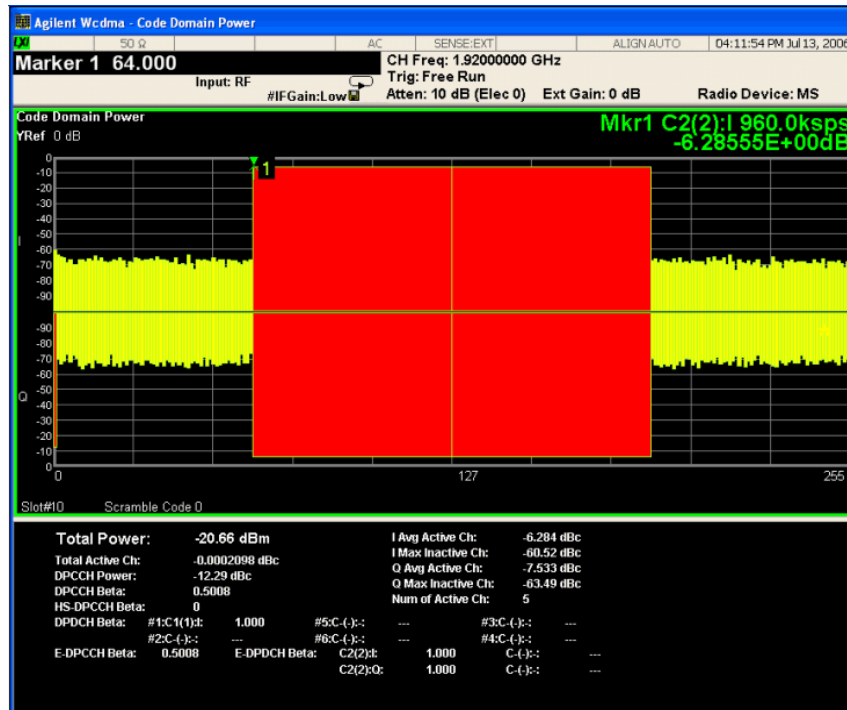
Step 7. Press **Marker ->**, **Mkr-> Despread** to initiate the despreading and decoding of the marked channel to allow EVM and other error measurements to be conducted on the channel.

Step 8. Press **View/Display**, **Code Domain (Quad View)** to display a combination view of the code domain power, symbol power, and I/Q symbol polar vector graph windows, with a summary results window. See Figure 8-4.

Figure 8-4   **Code Domain Measurement Result - Code Domain Quad View**
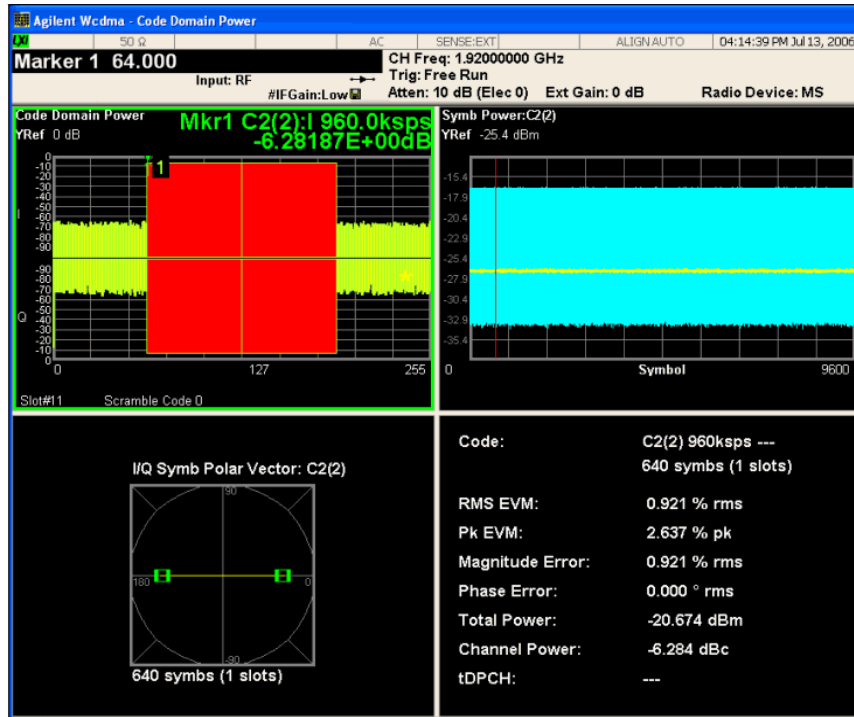
The original Code Domain Measurement is shown at the top left, while the Symbol Power measurement of the marked I-data channel is at the top right. The solid area below the first gradicule (blue on the instrument display) is the composite chip power versus time over the entire capture interval, while the (yellow) horizontal line is symbol power versus time for C2(2). The Capture Interval is 1 frame, but the measured interval is 1 slot.

The graph of the I/Q vector trajectory for C2(2) during the measurement interval is shown at lower left. As the constellation diagram shows, this example uses I-only data that is effectively BPSK modulation for channel C2(2), so the phase error must be zero.

The summary data at the lower right indicates peak and RMS EVM, magnitude and phase errors, powers of the signal and the channel.

Step 9. Press **View/Display**, **I/Q Error (Quad View)** to display a combination view of the magnitude error vs. symbol, phase error vs. symbol, and EVM vs. symbol graph windows, with the modulation summary results window. See Figure 8-5.

Figure 8-5 **Code Domain Measurement Result - I/Q Error Quad View**
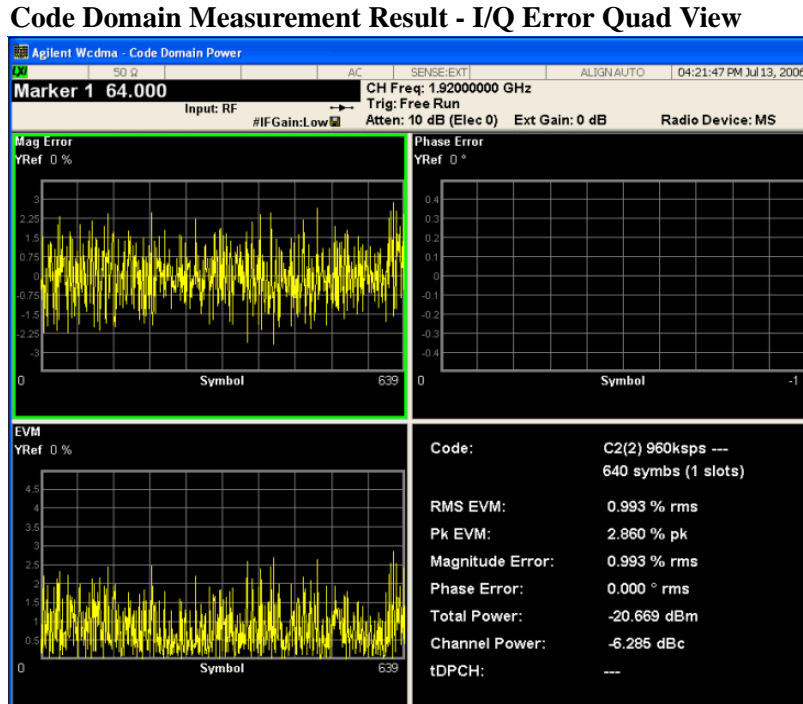
The results screen shows the data for the same code domain channel C2(2) that was selected for despreading by the marker in the Code Domain Quad View in the previous step.

Again, this example uses I-only data that is effectively BPSK modulation for channel C2(2), the phase error must therefore be zero.

Step 10. Press **View/Display, Demod Bits** to display a combination view of the code domain power, symbol power graph windows, and the I/Q demodulated bit stream data for the symbol power slots selected by the measurement interval and measurement offset parameters.

Figure 8-6   **Code Domain Measurement Result - Demod Bits View**
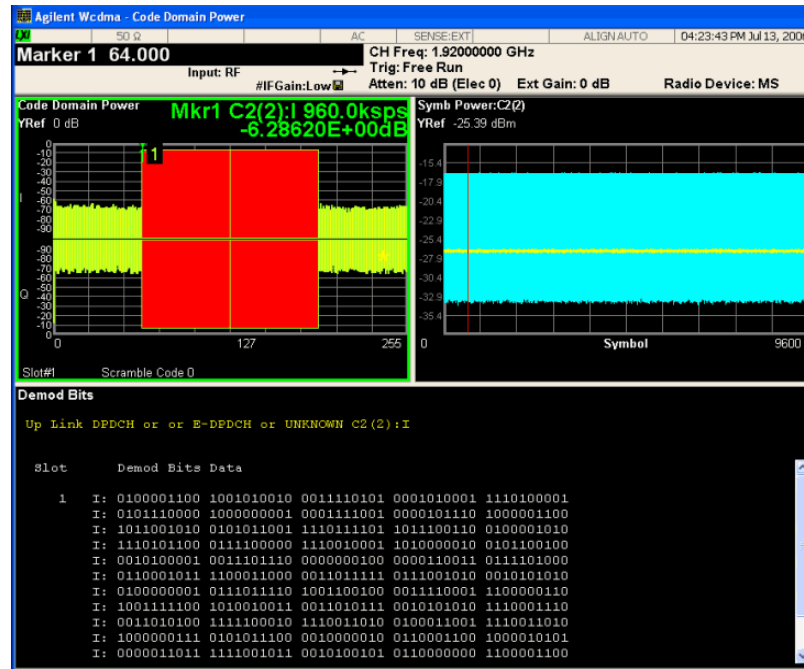
The Demod Bits View displays the same Code Domain Power and Symbol Power windows as the Code Domain (Quad View) shown in .

The demodulated bit stream displayed is the data contained in the Measurement Interval, slot #1. In the Symbol Power graph, this is the data between the red vertical lines; 1 slot, with no offset, so it is the first slot of the capture interval of 1 frame.

If you have a problem, and get an error message, see the "*Error Messages Guide*".

HSDPA DL Measurement Example (Test Model 5)

Configuring the Measurement System

Use the system controller to remotely control the base transceiver station (BTS) under test to transmit the RF power. The W-CDMA modulated interference signal is injected to the antenna output port of the BTS through an attenuator and circulator. The transmitting signal from the BTS is connected to the RF input port of the instrument from the circulator port. Connect the equipment as shown.

Figure 8-7 **Intermodulation Product Measurement System**
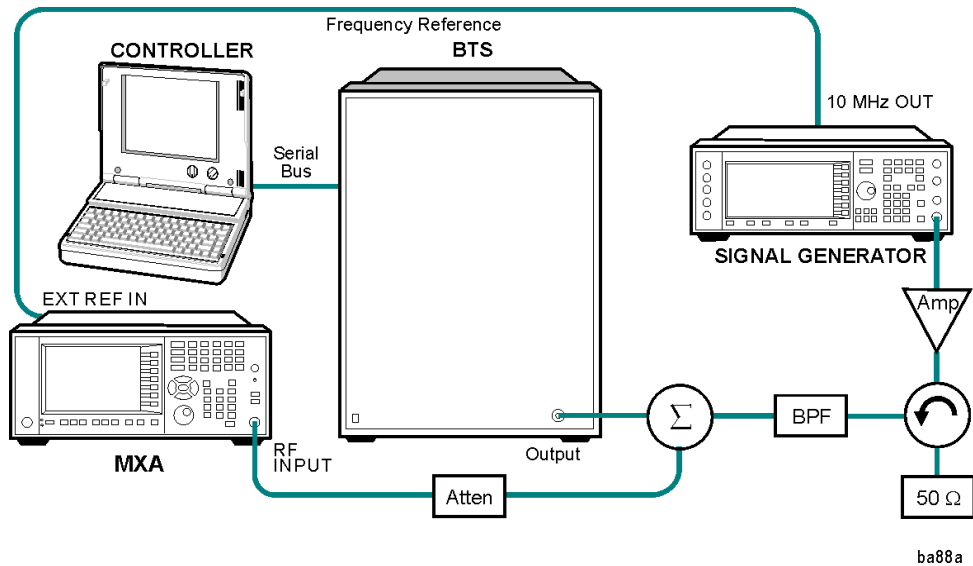
1. Using the appropriate amplifier, circulator, bandpass filter, combiner, cables, and adapters, connect the unmodulated carrier signal from the signal generator to the output connector of the BTS.

2. Connect the circulator output signal to the RF input port of the analyzer through the attenuator.

3. Connect a BNC cable between the 10 MHz OUT port of the signal generator and the EXT REF IN port of the analyzer.

4. Connect the system controller to the BTS through the serial bus cable.

Setting the BTS (Example)

From the BTS simulator or the system controller, or both, perform all of the call acquisition functions required for the BTS to transmit the RF power as follows:

Frequency: 1000 MHz

Physical Channels: Test Model 5 with 8 HS-PDSCH

Scramble Code: 0

Output Power: –10 dBm

Measurement Procedure

Step 1. Press **Mode**, **W-CDMA with HSDPA/HSUPA** to enable the W-CDMA w/HSDPA/HSUPA measurements.

Step 2. Press **Mode Preset** to preset the mode.

Step 3. Press **Mode Setup**, **Radio**, **Device** to toggle the device to **BTS**.

Step 4. Press **FREQ Channel**, **1000**, **MHz** to set the center frequency to 1.000 GHz.

Step 5. Press **Meas**, **Code Domain** to initiate the code domain measurement.

Step 6. Press **Meas Setup**, **Symbol Boundary**, **Predefined Test Models**, **Test Model 5**, **Test Model 5 w/ 8 HS-PDSCH w/30 DPCH**.

Figure 8-8 **Code Domain Measurement Result - Power Graph & Metrics (Default) View - Downlink (BTS) Test Model 5**
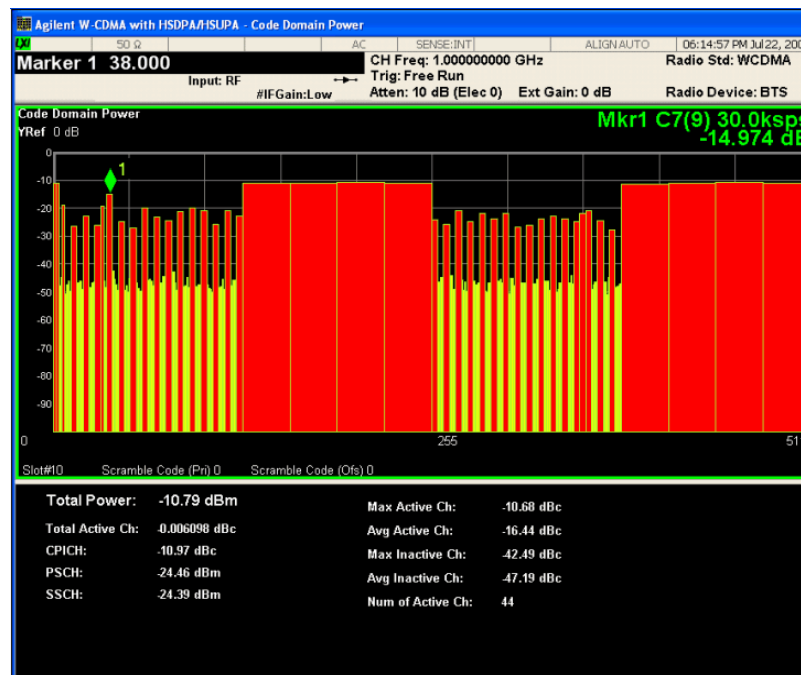
The Code Domain Power measurement result should look similar to Figure 8-8. The graph window is displayed with a text window below it. The text window shows the total power level along with the relative power levels of the various channels.

Now to examine a single HSDPA code channel in the code domain more closely:

Step 7. Press **Marker**, and enter **38** using the front panel keypad, **Enter**.

Step 8. Press **Marker**, **Mkr->**, **Mkr-> Despread** to initiate the despreading and decoding of the marked channel to allow EVM and other error measurements to be conducted on the channel.

Step 9. Press **View/Display**, **Code Domain** (**Quad View**) to display the combination view of the code domain power, symbol power, and I/Q symbol polar vector graph windows, and summary results window. See Figure 8-9.

Figure 8-9   **Code Domain Measurement Result - Code Domain Quad View - HSDPA DL Test Model 5**
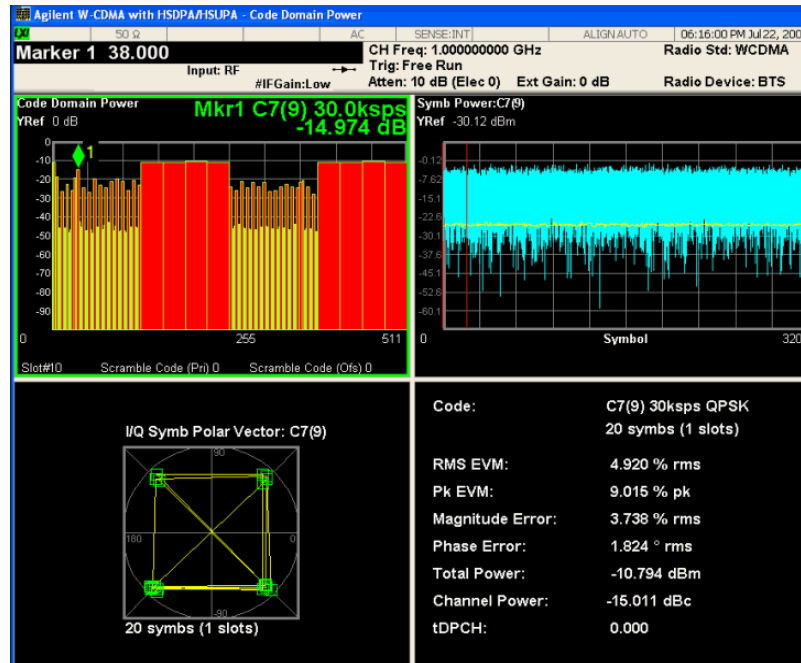
The original Code Domain Measurement with the marker at code channel 38 is shown at the top left, while the Symbol Power measurement of the marked channel is at the top right. The solid area below the first gradicule (blue on the instrument display) is the composite chip power over the entire capture interval, while the (yellow) horizontal line is Symbol power for C7(9).

The vertical red line in the graph indicates the measurement interval, with the default measurement offset of 0 slots. The graph of the I/Q vector trajectory for C7(9) during the measurement interval is shown at lower left. The summary data at lower right indicates peak and RMS EVM, magnitude and phase errors, powers of signal and channel.

TIP   If your EVM or Phase Error results are high, and you have many code channels in your signal, try using the Multi Channel Estimator to improve your measurement result. Press **Meas Setup**, **Advanced,** and toggle the **Multi Channel Estimator** key to **ON**.

Step 10. Press **View/Display**, **Demod Bits** to display the combination view of the code domain power, symbol power graph windows, and the I/Q demodulated bit stream data for the symbol power slots selected by the measurement interval and measurement offset parameters.

Figure 8-10   **Code Domain Measurement Result - Demod Bits View - HSDPA DL Test Model 5**
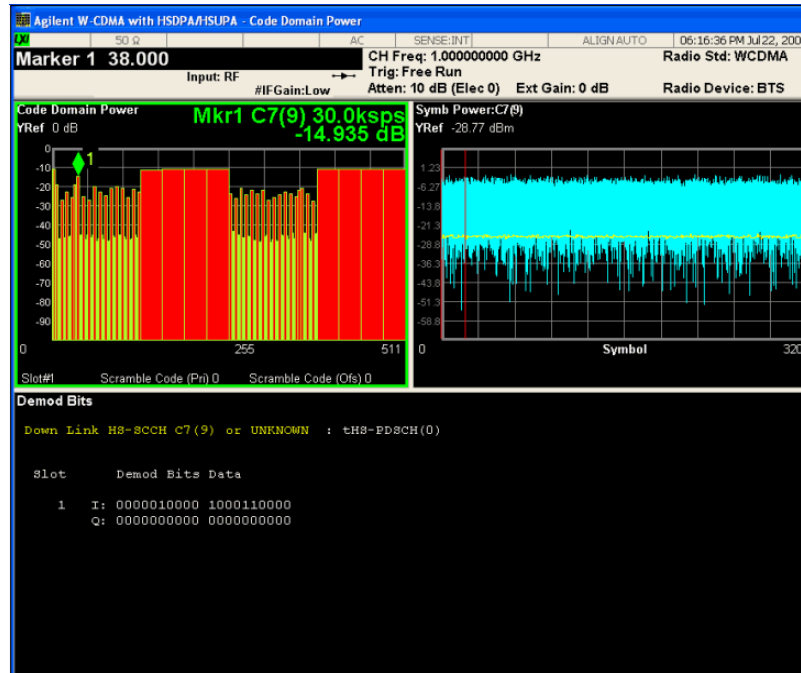
The Demod Bits View displays the same Code Domain Power and Symbol Power windows as the Code Domain (Quad View) shown in Figure 8-9 on page 46.

The demodulated bit stream displayed is the data contained in the Measurement Interval (1 slot, with no offset, so it is the first slot) of the Capture Interval of 2 frames.

Step 11. Press **View/Display**, **Power Graph & Metrics** to display the primary code domain power view and summary results window for another HSDPA code channel, HS-PDCSH.

Step 12. Press **Marker**, and enter **140** using the front panel keypad, **Enter**.

Step 13. Press **Mkr->, Mkr-> Despread** to initiate the despreading and decoding of the marked channel to allow EVM and other error measurements to be conducted on the channel. It may be necessary to press **Restart** if the measurement setting is on **Single**.

Step 14. Press **View/Display**, **Code Domain** (**Quad View**) to display the combination view of the code domain power, symbol power, and I/Q symbol polar vector graph windows, and summary results window.

Figure 8-11   **Code Domain Measurement Result - Code Domain Quad View - HSDPA DL Test Model 5**
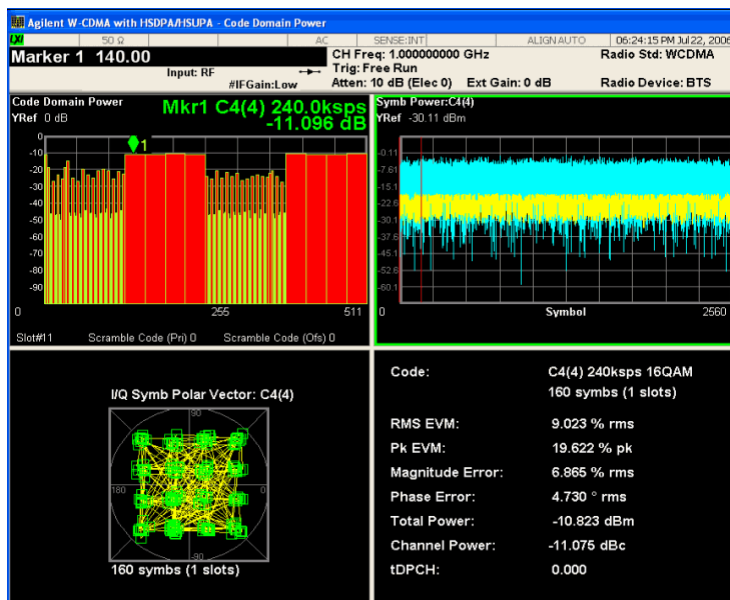
This code channel C4(4) is the HS-PDSCH, unique to HSDPA, and present in Test Model 5. The difference in symbol power can be clearly seen. The 16QAM modulation is also displayed, instead of the normal QPSK for W-CDMA DPCH channels.

Step 15. Press **View/Display**, **Demod Bits** again to display the I/Q demodulated bit stream data for the symbol power slots selected by the measurement interval and measurement offset parameters.

Figure 8-12   **Code Domain Measurement Result - Demod Bits View (Binary)**
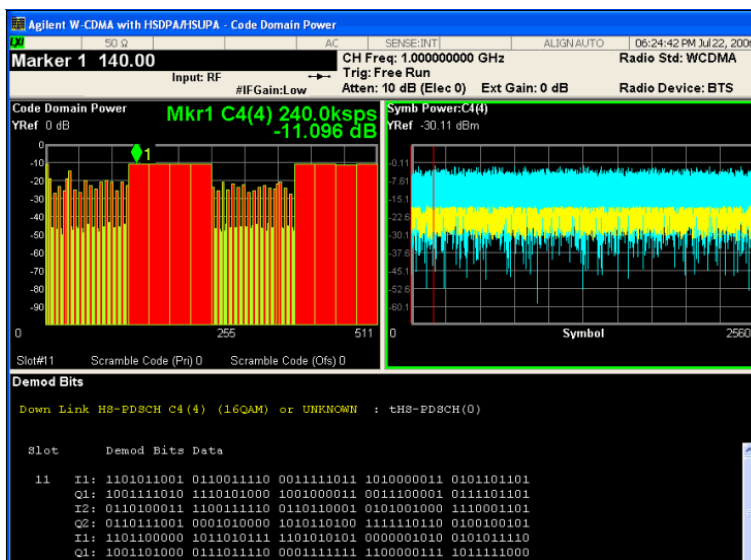
The demodulated bits for slot 11 are shown in Binary format. You can also view the bit stream in Hexadecimal format by doing the following:

Using the Next Window key, move the view to the Demod Bits screen.
Press **View/Display**, **Demod Bits**, **Demod Bits Format** to toggle to Hex format

If you have a problem, and get an error message, see the "*Error Messages Guide*".

Troubleshooting Hints

Uncorrelated interference may cause CW interference like local oscillator feed through or spurs. Another cause of uncorrelated noise can be I/Q modulation impairments. Correlated impairments can be due to the phase noise on the local oscillator in the upconverter or I/Q modulator of the unit under test (UUT). These will be analyzed by the code domain measurements along with the QPSK EVM measurements and others.

Poor phase error indicates a problem at the I/Q baseband generator, filter, or modulator in the transmitter circuitry of the UUT, or both. The output amplifier in the transmitter can also create distortion that causes unacceptably high phase error. In a real system, poor phase error will reduce the ability of a receiver to correctly demodulate the received signal, especially in marginal signal conditions.

9   Modulation Accuracy (Composite EVM) Measurements

This section explains how to make the modulation accuracy (composite EVM) measurement on a W-CDMA mobile station (MS). Modulation accuracy is the ratio of the correlated power in a multi-coded channel to the total signal power.

Setting Up and Making a Measurement

Configuring the Measurement System

The MS under test must be set to transmit the RF power remotely through the system controller. This transmitting signal is connected to the RF input port of the instrument. Connect the equipment as shown.

Figure 9-1　　　　　**Modulation Accuracy Measurement System**

1. Using the appropriate cables, adapters, and circulator, connect the output signal of the MS to the RF input of the analyzer.

2. Connect the base transceiver station simulator or signal generator to the MS through the circulator to initiate a link constructed with the sync and pilot channels, if required.

3. Connect a BNC cable between the 10 MHz OUT port of the signal generator and the EXT REF IN port of the analyzer.

4. Connect the system controller to the MS through the serial bus cable to control the MS operation.

Setting the MS (Example)

From the base transceiver station simulator or the system controller, or both, perform all of the call acquisition functions required for the MS to transmit the RF power as follows:

Frequency:　　　　　　　1920 MHz (Channel Number: $5 \times 1,920 = 9,600$)

Physical Channels:　　　A coded signal with the DPCCH and at least one DPDCH is required to make a composite EVM measurement on a W-CDMA UL signal. (A W-CDMA DL signal must

contain either the SCH or the CPICH.)

Scramble Code: 0

Output Power: –20 dBm (at analyzer input)

Measurement Procedure

Step 1. Press **Mode**, **W-CDMA with HSDPA/HSUPA** to enable the W-CDMA measurements.

Step 2. Press **Preset** to preset the mode.

Step 3. Press **Mode Setup**, **Radio**, **Device** to toggle the device to **MS**.

Step 4. Press **FREQ Channel**, **1920**, **MHz** to set the center frequency to 1.920 GHz.

Step 5. Press **Meas**, **Mod Accuracy (Composite EVM)** to initiate the modulation accuracy (composite EVM) measurement.

The Mod Accuracy I/Q Polar Vector Constellation measurement result should look similar to Figure 9-2.

Figure 9-2   **Modulation Accuracy Measurement Result - I/Q Measured Polar Graph (Default) View**
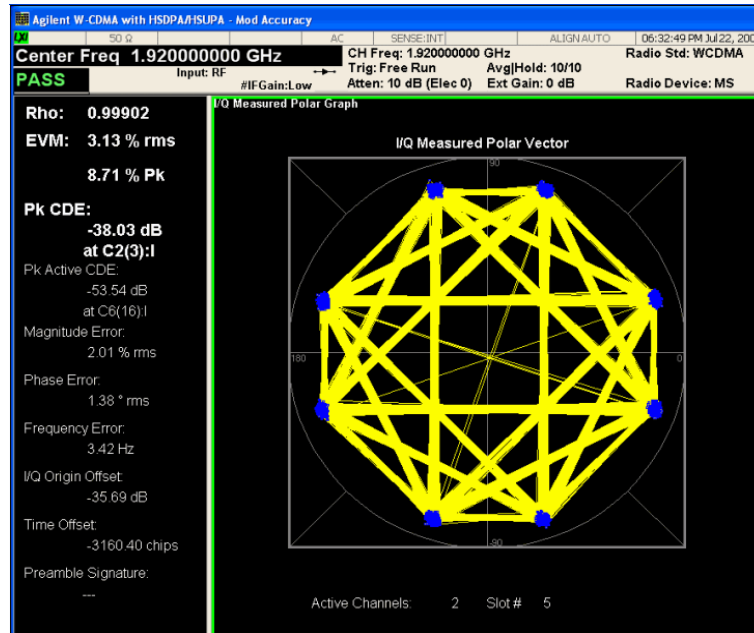
The modulation constellation is shown, along with summary data for Rho, EVM, Peak Code Domain Error, and phase and magnitude errors.

Step 6. Press **View/Display**, **I/Q Measured Polar Graph, I/Q PolarVec/Constln, Constellation** to display a view of the I/Q measured polar constellation graph window and the modulation summary result window.

Figure 9-3 **Modulation Accuracy Measurement Result - Polar Constellation View**
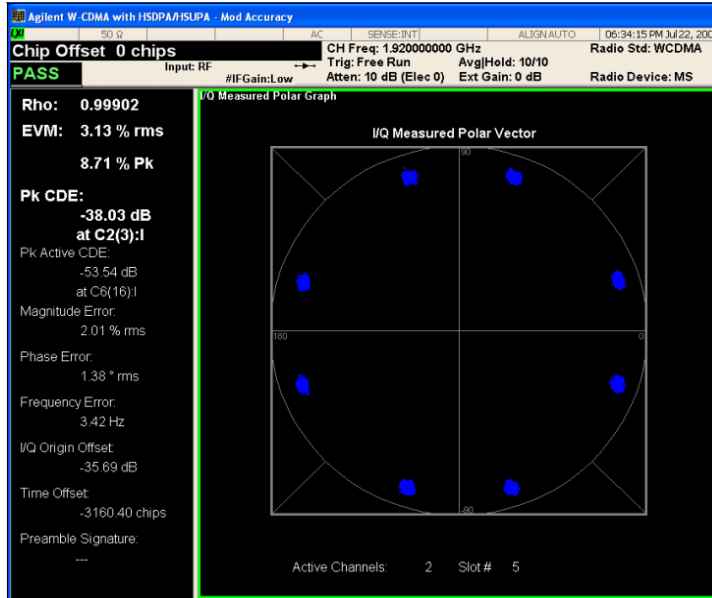
Step 7. Press **View/Display**, **I/Q Error** to display a combination view of the magnitude error, phase error, and EVM graph windows.

Figure 9-4 **Modulation Accuracy Measurement Result - I/Q Error View**
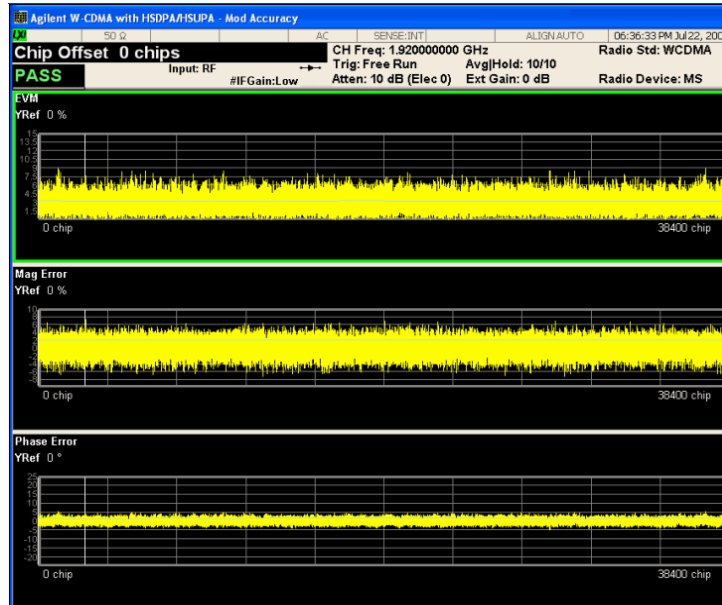
If you have a problem, and get an error message, see the "*Error Messages Guide*".

Troubleshooting Hints

A poor phase error often indicates a problem with the I/Q baseband generator, filters, or modulator, or all three, in the transmitter circuitry of the unit under test (UUT). The output amplifier in the transmitter can also create distortion that causes unacceptably high phase error. In a real system, a poor phase error will reduce the ability of a receiver to correctly demodulate the received signal, especially in marginal signal conditions.

If the error "Can not correlate to input signal" is shown, it means that your measurement has failed to find any active channels due to the lack of correlation with the input signal. The input signal level or scramble code, or both, may need to be adjusted to obtain correlation.

10 Power Control Measurements

This chapter explains how to make power control measurements on W-CDMA mobile stations (MS). Power control measurements characterize the ability of a mobile station to vary the power levels of a digitally modulated signal, as directed by the base station. There are three selections of measurement type; Slot Power to monitor the power steps, PRACH Power to verify the PRACH preambles and PRACH message power levels, and Slot Phase for user equipment (UE) phase discontinuity.

Setting Up and Making a Measurement

Configuring the Measurement System

The MS under test must be set to transmit the RF power remotely through the system controller. This transmitting signal is connected to the RF input port of the instrument. Connect the equipment as shown.

Figure 10-1   **Power Control Measurement System**
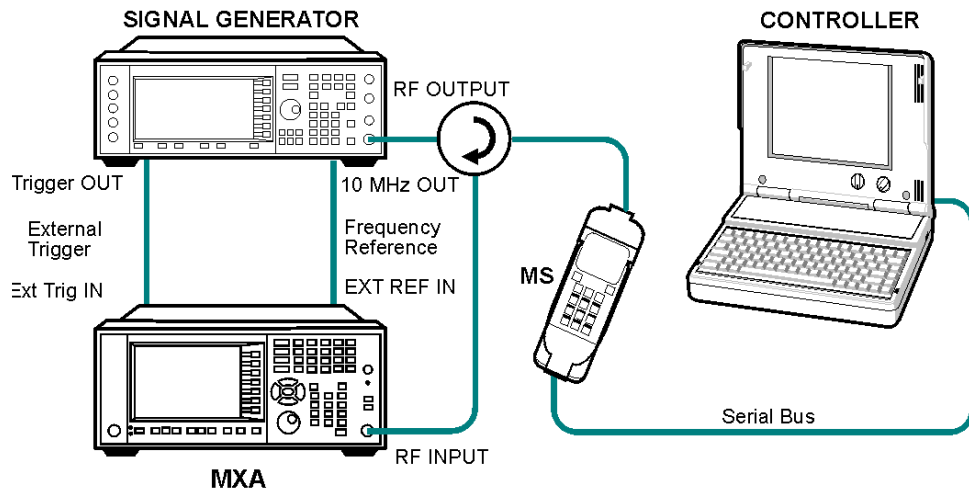
1. Using the appropriate cables, adapters, and circulator, connect the output signal of the MS to the RF input of the analyzer.

2. Connect the base transceiver station simulator or signal generator to the MS through the circulator to initiate a link constructed with the sync and pilot channels, if required.

3. Connect a BNC cable between the 10 MHz OUT port of the signal generator and the EXT REF IN port of the analyzer.

4. Connect a trigger signal from the signal generator or system controller and the EXT TRIG IN port of the analyzer.

5. Connect the system controller to the MS through the serial bus cable to control the MS operation.

Setting the MS

From the transceiver station simulator or the system controller, or both, perform all of the call acquisition and power control functions required for the MS to transmit the RF power as follows:

Frequency: 1000 MHz

Physical Channels: DPCCH with one or more DPDCH

NOTE   This example shows a signal with 4 dB power steps across the frame.

Output Power: –15 dBm (at analyzer input) peak

Measurement Procedure

Step 1. Press **Mode**, **W-CDMA with HSDPA/HSUPA** to enable the W-CDMA measurements.

Step 2. Press **Mode Preset** to preset the mode.

Step 3. Press **Mode Setup**, **Radio**, **Device** to toggle the device to **MS**.

Step 4. Press **Trigger** to select the **External 1** or **External 2** trigger supplied.

Step 5. Press **FREQ Channel**, **1000**, **MHz** to set the center frequency to 1.000 GHz.

Step 6. Press **Meas**, **Power Control** to initiate the default power control measurement

The default power control measurement result should look similar to Figure 10-2.

Figure 10-2   **Power Control Measurement Result - Slot Power Graph Metrics View**
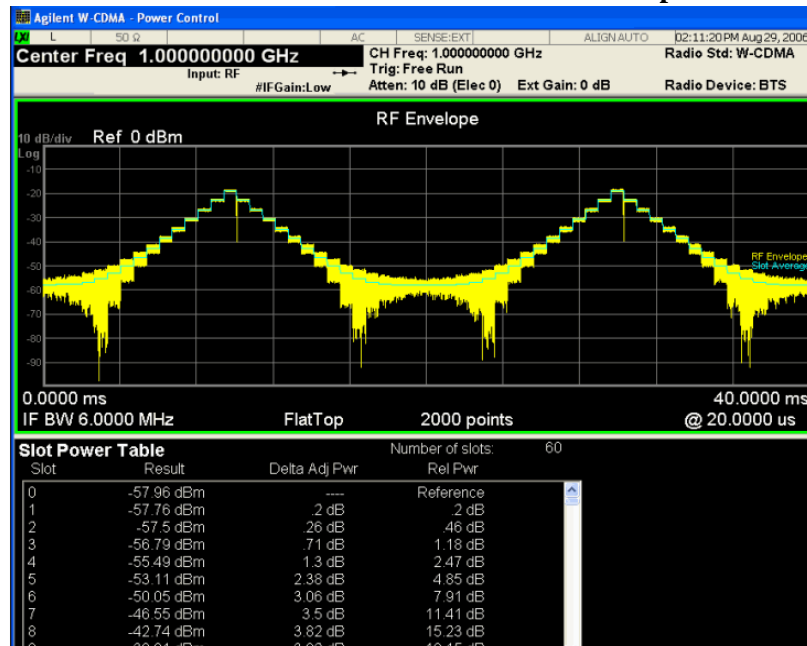
Figure 10-3 **Power Control Measurement Result - PRACH Power Graph Metrics View**
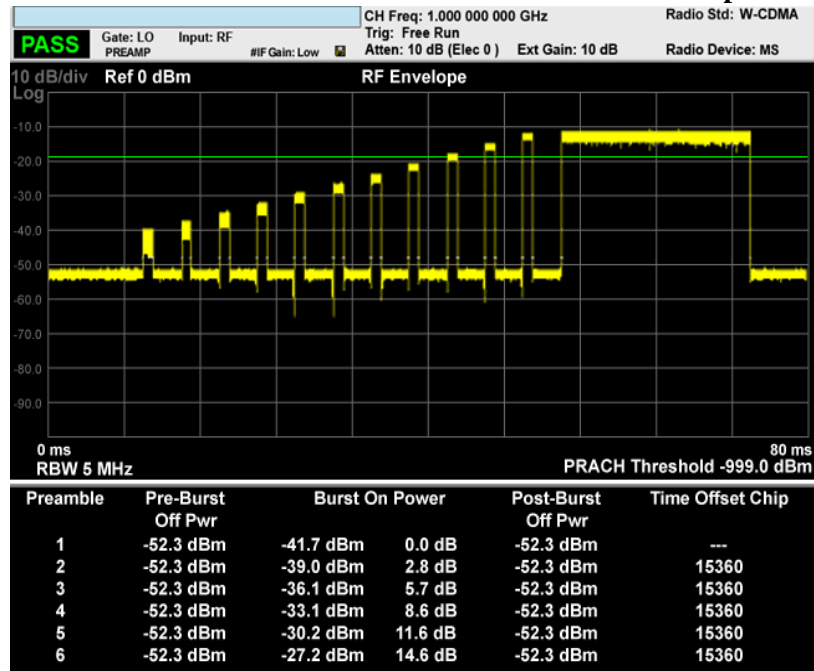
Figure 10-4 **Power Control Measurement Result - Slot Phase Power Graph Metrics View**
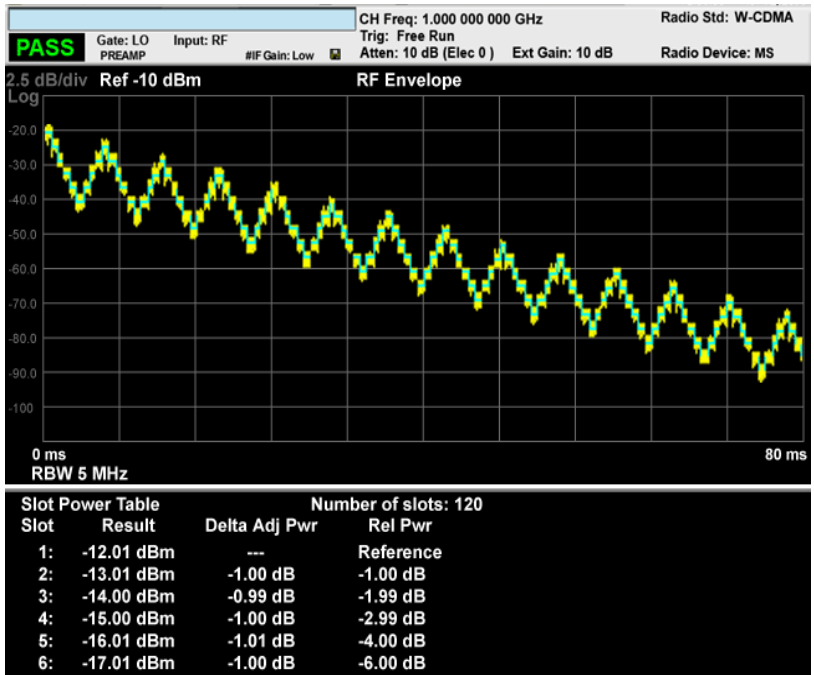
Figure 10-5   **Power Control Measurement Result - Slot Phase Graph Metrics View**

Step 7. To make measurements repeatedly, press the **Cont** front panel key.

If you have a problem, and get an error message, see the "*Error Messages Guide*".

Troubleshooting Hints

The power control measurement, along with the power versus time measurement and spectrum measurement, can reveal the effects of degraded or defective parts in the transmitter section of the unit under test (UUT). The following are areas of concern which can contribute to performance degradation:

• DC power supply control of the transmitter power amplifier, RF power control of the pre-power amplifier stage, or I/Q control of the baseband stage, or all.

• Gain and output power levels of the power amplifier, caused by degraded gain control or increased distortion, or both.

• Amplifier linearity.

11   QPSK EVM Measurements

This chapter explains how to make the QPSK error vector magnitude (EVM) measurement on a W-CDMA mobile station (MS). QPSK EVM is a measure of the phase and amplitude modulation quality that relates the performance of the actual signal compared to an ideal signal as a percentage, calculated over the course of the ideal constellation.

Setting Up and Making a Measurement

Configuring the Measurement System

The mobile station (MS) under test must be set to transmit the RF power remotely through the system controller. This transmitting signal is connected to the RF input port of the instrument. Connect the equipment as shown.

Figure 11-1   **QPSK EVM Measurement System**
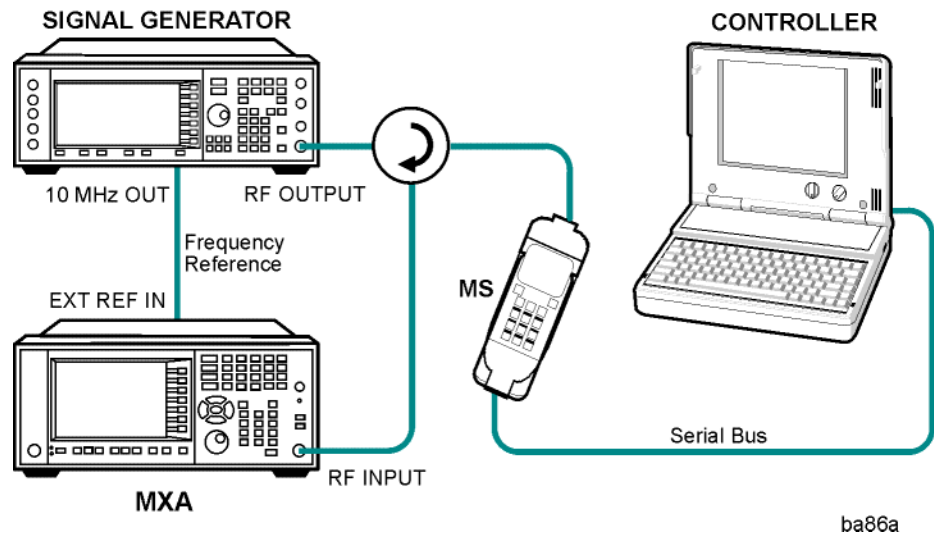
1. Using the appropriate cables, adapters, and circulator, connect the output signal of the MS to the RF input of the analyzer.

2. Connect the base transceiver station simulator or signal generator to the MS through the circulator to initiate a link constructed with the sync and pilot channels, if required.

3. Connect a BNC cable between the 10 MHz OUT port of the signal generator and the EXT REF IN port of the analyzer.

4. Connect the system controller to the MS through the serial bus cable to control the MS operation.

Setting the MS

From the base transceiver station simulator or the system controller, or both, perform all of the call acquisition functions required for the MS to transmit the RF power as follows:

Frequency: 1920 MHz (Channel Number: $5 \times 1{,}920 = 9{,}600$)

Physical Channels: DPCCH only

Scramble Code: 0

Output Power: –20 dBm (at analyzer input)

Measurement Procedure

Step 1. Press **Mode**, **W-CDMA with HSDPA/HSUPA** to enable the W-CDMA measurements.

Step 2. Press **Mode Preset** to preset the mode.

Step 3. Press **Mode Setup**, **Radio**, **Device** to toggle the device to **MS**.

Step 4. Press **FREQ Channel**, **1920**, **MHz** to set the center frequency to 1.920 GHz.

Step 5. Press **Meas, QPSK EVM** to initiate the QPSK EVM measurement.

The QPSK EVM I/Q Measured Polar Vector measurement result should look similar to Figure 11-2. The measurement values for modulation accuracy are shown in the summary result window.

Figure 11-2   **QPSK EVM Result - Polar Vector/Constellation (Default) View**
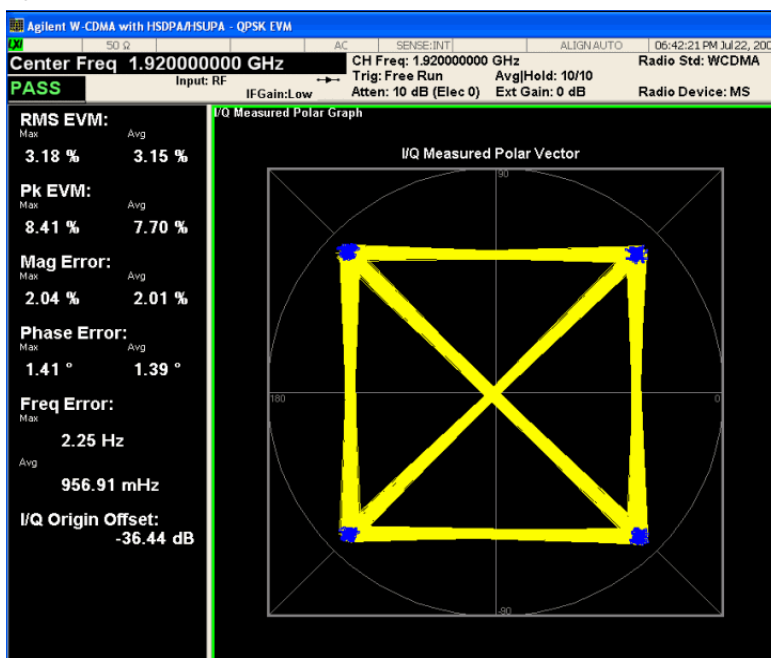
Step 6. Press **View/Display**, **I/Q Measured Polar Graph**, **I/Q Polar Vec/Constln**, **Constellation** to display a view of the I/Q measured polar constellation graph window and the modulation summary result window.

Figure 11-3   **QPSK EVM Result - Polar Constellation View**
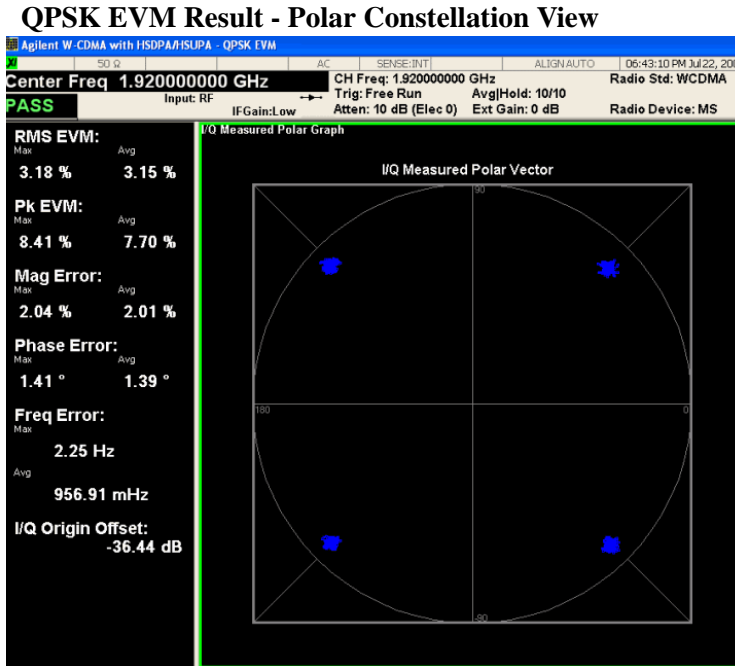
Step 7. Press **View/Display**, **I/Q Error** to display a combination view of the magnitude error, phase error, EVM graph windows, and the modulation summary result window.

Figure 11-4   **QPSK EVM Result - I/Q Error Quad View**
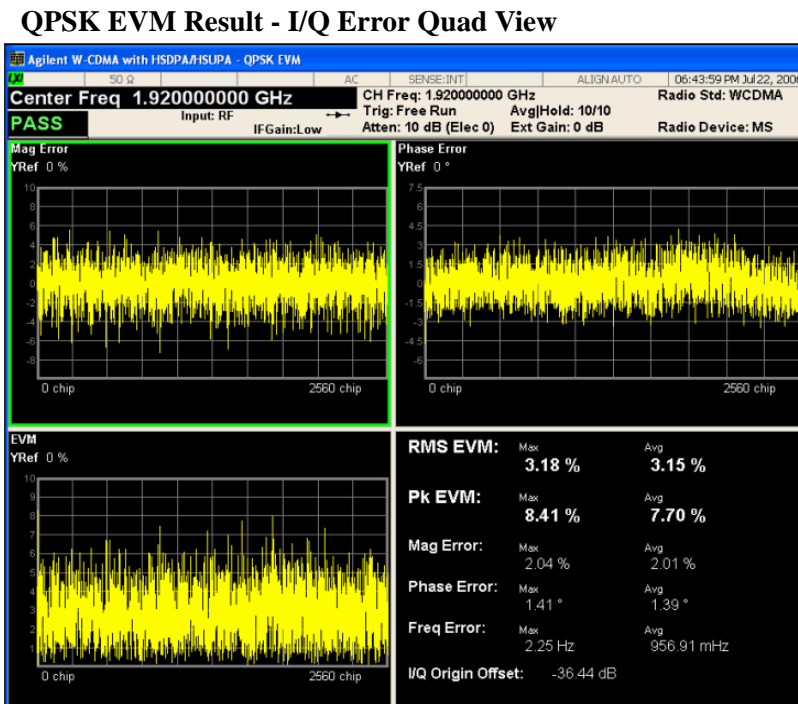
If you have a problem, and get an error message, see the "*Error Messages Guide*".

Troubleshooting Hints

A poor phase error indicates a problem with the I/Q baseband generator, filters, or modulator, or all, in the transmitter circuitry of the unit under test (UUT). The output amplifier in the transmitter can also create distortion that causes unacceptably high phase error. In a real system, a poor phase error will reduce the ability of a receiver to correctly demodulate the received signal, especially in marginal signal conditions.

QPSK EVM Measurements

12   Monitor Spectrum Measurements

This chapter explains how to make a Monitor Spectrum measurement on a signal source. Monitor Spectrum measurements show a spectrum domain display of the signal.

Setting Up and Making a Measurement

Configuring the Measurement System

This example shows a signal generator test set up to transmit RF power. The transmitting signal is connected to the RF input port of the analyzer. Connect the equipment as shown.

Figure 12-1   **Monitor Spectrum Measurement**
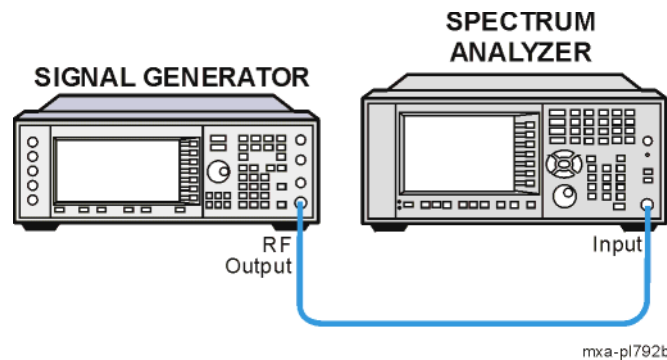
1. Using the appropriate cables and adapters, connect the output signal of the signal generator to the RF input of the analyzer.

2. For best frequency accuracy, connect a BNC cable between the 10 MHz REF IN port of the signal generator (if available) and the 10 MHz EXT REF OUT port of the analyzer.

Measurement Procedure

Step 1. Setup the signal source as follows:

Set the mode to W-CDMA 3GPP
Set the frequency 1.0 GHz.
Set the amplitude to –10 dBm.

Step 2. Connect the source RF OUTPUT to the analyzer RF INPUT as shown in Figure 12-1.

Step 3. Enable the W-CDMA mode:

Press **Mode**, **W-CDMA with HSPA**.

Step 4. Preset the analyzer mode:

Press **Mode Preset**.

Step 5. Set the measurement center frequency:

Press **FREQ Channel**, enter a numerical frequency using the front-panel keypad, and select a units key, such as **MHz**.

Step 6. Set the measurement span frequency:

Press **SPAN X Scale**, enter a numerical span using the front-panel keypad, and select a units key, such as **MHz**.

Step 7. Initiate the measurement:

Press **Meas**, **Monitor Spectrum**.

NOTE   A display with a Spectrum window appears when you activate a Spectrum measurement. Changes to the **FREQ**, **Span**, or **AMPTD** settings will affect only the active window.

The default display shows the **Current** (yellow trace) data. To make viewing the display easier, you can view either the **Current** trace or **Average** separately.

• Press **Trace/Detector, Select Trace** and select the trace(s) desired for display, then toggle **Display** to **Show**.

Figure 12-2   **Monitor Spectrum Measurement - Spectrum and I/Q Waveform (Default View)**
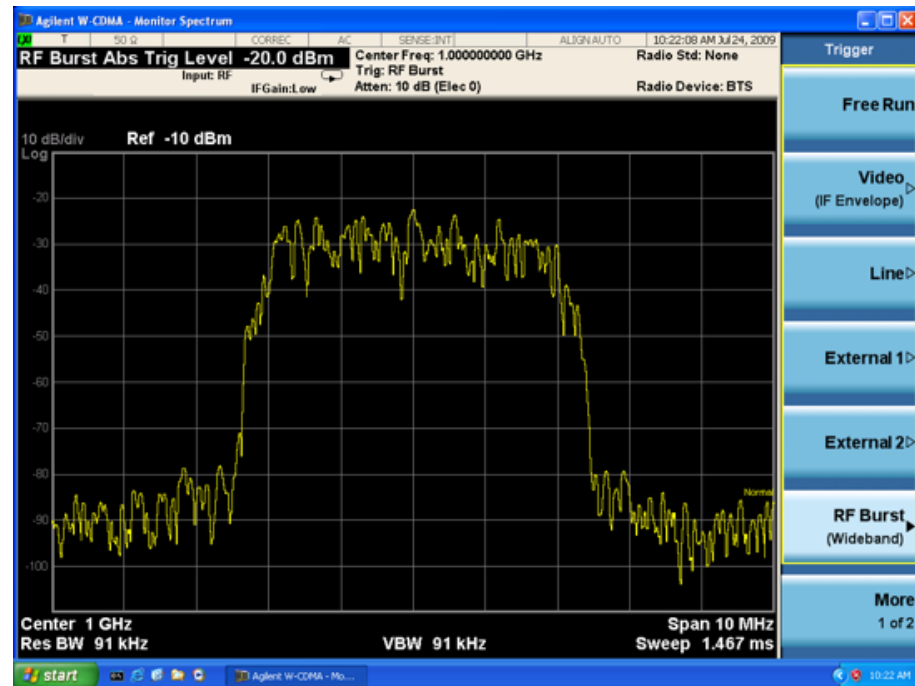
Step 8. To make a measurement repeatedly, press **Cont**.

13 IQ Waveform (Time Domain) Measurements

This chapter section explains how to make a waveform (time domain) measurement on a W-CDMA base transceiver station (BTS). The measurement of I and Q modulated waveforms in the time domain enables you to see the voltages which comprise the complex modulated waveform of a digital signal.

Setting Up and Making Measurements

Configuring the Measurement System

The BTS under test must be set to transmit the RF power remotely through the system controller. This transmitting signal is connected to the RF input port of the analyzer. Connect the equipment as shown. An interfering or adjacent signal may supplied as shown.

Figure 13-1   **Waveform Measurement System**

bts_test_setup
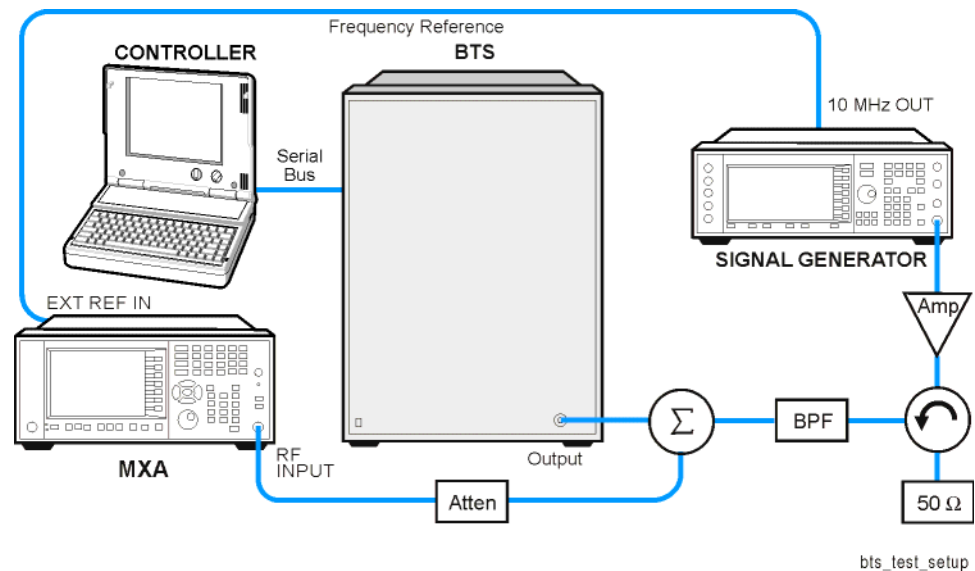
1. Using the appropriate cables, and circulator, connect the output signal of the BTS to the RF input of the analyzer.

2. Connect the base transmission station simulator or signal generator to the BTS through a circulator to initiate a link constructed with sync and pilot channels, if required.

3. For best frequency accuracy, connect a BNC cable between the 10 MHz OUT port of the signal generator and the EXT REF IN port of the analyzer.

4. Connect the system controller to the BTS through the serial bus cable to control the BTS operation.

5. Connect an external trigger, if needed. Press **Mode Setup**, **Trigger** to access a menu to set up inputs and levels for all triggers. You must then select the appropriate trigger under the **Meas Setup**, **Trigger** menu to direct the measurement to use your trigger settings.

Setting the BTS

From the base transceiver station simulator and the system controller, set up a call using loopback mode for the BTS to transmit the RF signal.

Measurement Procedure

Step 1. Set the analyzer to the appropriate mode and enable the W-CDMA mode measurements:

Press W-CDMA with HSDPA/HSUPA.

Step 2. Preset the analyzer mode:

Press **Mode Preset**.

Step 3. Set the measurement center frequency:

Press **FREQ Channel**, enter a numerical frequency using the front-panel keypad, and select a units key, for example **MHz**.

Step 4. Initiate the IQ Waveform measurement:

Press **Meas**, **IQ Waveform**.

Figure 1   **Waveform Measurement - RF Envelope (Default View)**
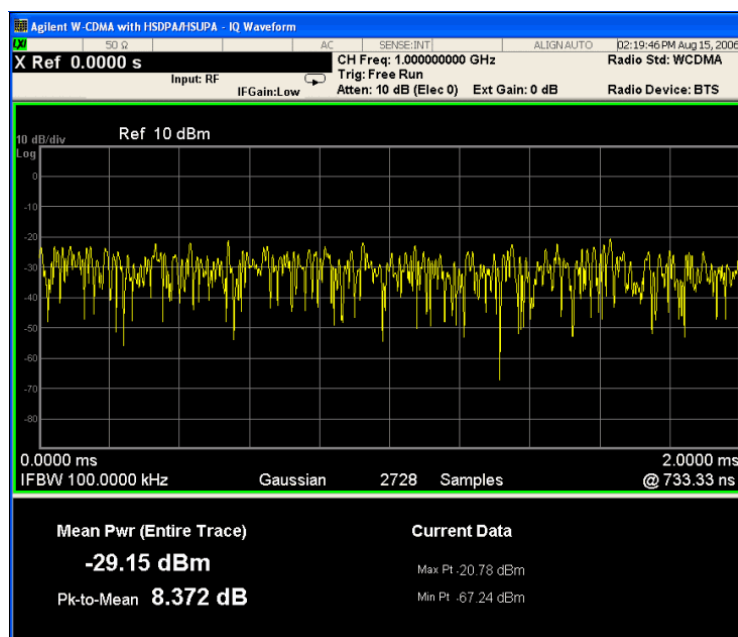
*Meas Setup: View/Display = RF Envelope View,
                         Others = Factory default settings

*Input signal: W-CDMA (3GPP 3.4 12-00), Test Model 1,

The default display shows the RF Envelope with the current data. The measured values for the mean power and peak-to-mean power are shown in the text window.

Step 5. Select the IQ Waveform view.

Press **View/Display, IQ Waveform** .

The IQ Waveform window provides a view of the I and Q waveforms together on the same graph in terms of voltage versus time in linear scale.

Figure 13-2   **Waveform Measurement - IQ Waveform View**
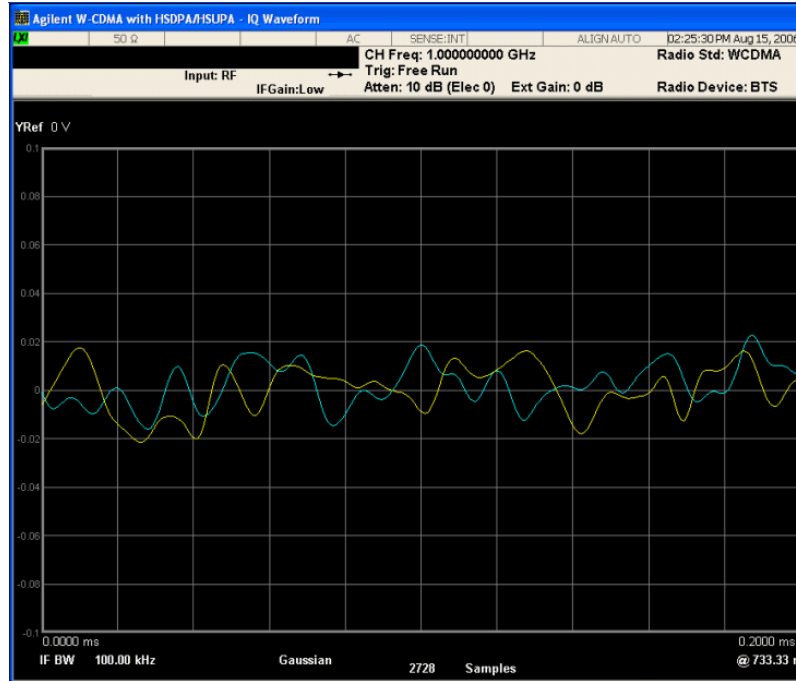
*Meas Setup: View/Display = IQ Waveform View,
                            Others = Factory defaults, except X and Y scales

*Input signal: W-CDMA (3GPP 3.4 12-00), Test Model 1,

Step 6. Press **Marker**, **Properties**, **Marker Trace**, **I/Q Waveform** to activate a marker on the I/Q Waveform trace. Rotate the knob until the marker is shown at a desired time in the waveform for viewing the trace values at the time position of the marker.

Step 7. To make a measurement repeatedly, press **Cont**.

Step 8. Press **Meas Setup** to see the keys available to change the measurement parameters from the default condition.

Using the Waveform Measurement to Set Up Triggering (for burst signals)

You can use the waveform measurement to view your signal in the time domain and to help select the appropriate trigger to acquire your signal.

Step 1. Activate the waveform measurement view:

Press **Meas**, **IQ Waveform**.

Step 2. Adjust the scale of the x-axis to view the complete signal waveform:

Press **SPAN X Scale**, **Scale/Div**, then use the front-panel keypad to input the scale/div, then press a units key, for example μ**s**, to complete the entry.

Step 3. Select a trigger source (free run is the default setting):

Press **Trigger**, then select one of the available trigger sources. You can also setup trigger holdoff and auto trigger timing.

Figure 13-3   **Waveform Measurement - RF Envelope View**

Figure 13-4   **Waveform Measurement- IQ Waveform View**
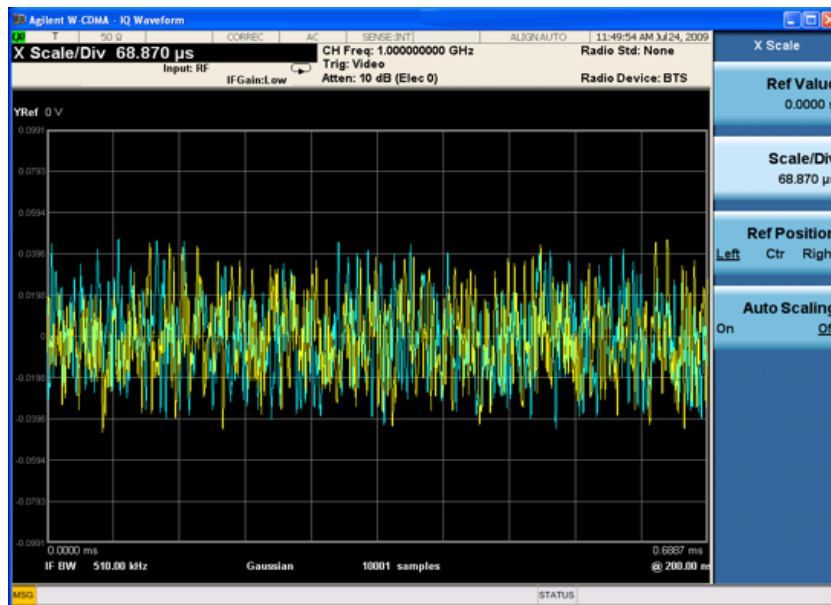
14 Making Time-Gated Measurements

Generating a Pulsed-RF FM Signal

Traditional frequency-domain spectrum analysis provides only limited information for certain signals. Examples of these difficult-to-analyze signal include the following:

- Pulsed-RF
- Time multiplexed
- Interleaved or intermittent
- Time domain multiple access (TDMA) radio formats
- Modulated burst

The time gating measurement examples use a simple frequency-modulated, pulsed-RF signal. The goal is to eliminate the pulse spectrum and then view the spectrum of the FM carrier as if it were continually on, rather than pulsed. This reveals low-level modulation components that are hidden by the pulse spectrum.

When performing these measurements you can use a digitizing oscillascope or your Agilent X-Series Signal Analyzer (using Gate View) to setup the gated signal. Refer back to these first three steps to setup the pulse signal, the pulsed-RF FM signal and the oscilloscope settings when performing the gated LO procedure (page 88), the gated video procedure (page 91) and gated FFT procedure (page 94).

For an instrument block diagram and instrument connections see "Connecting the Instruments to Make Time-Gated Measurements" on page 86.

Step 1. Setup the pulse signal with a period of 5 ms and a width of 4 ms:

There are many ways to create a pulse signal. This example demonstrates how to create a pulse signal using a pulse generator or by using the internal function generator in the ESG. See Table 14-1. if you are using a pulse generator or Table 14-2.if you are using a second ESG. Select either the pulse generator or a second ESG to create the pulse signal.

Table 14-1. 81100 Family Pulse Generator Settings

Period	5 ms (or pulse frequency equal to 200 Hz)
Pulse width	4 ms
High output level	2.5 V
Waveform	pulse
Low output level	-2.5 V
Delay	0 or minimum

Table 14-2. ESG #2 Internal Function Generator (LF OUT) Settings

LF Out Source	FuncGen
LF Out Waveform	Pulse
LF Out Period	5 ms
LF Out Width (pulse width)	4 ms
LF Out Amplitude	2.5 Vp
LF Out	On
RF On/Off	Off
Mod On/Off	On

Step 2. Set up ESG #1 to transmit a pulsed-RF signal with frequency modulation. Set the FM deviation to 1 kHz and the FM rate to 50 kHz:

ESG #1 generates the pulsed FM signal by frequency modulating the carrier signal and then pulse modulating the FM signal. The pulse signal created in step 1 is connected to the `EXT 2 INPUT` (on the front of ESG #1). The ESG `RF OUTPUT` is the pulsed-RF FM signal to be analyzed by the spectrum analyzer.

Table 14-3. ESG #1 Instrument Connections

Frequency	40 MHz
Amplitude	0 dBm
Pulse	On
Pulse Source	Ext2 DC
FM	On
FM Path	1
FM Dev	1 kHz
FM Source	Internal
FM Rate	50 kHz
RF On/Off	On
Mod On/Off	On

Step 3. If you are using your Agilent X-Series Signal Analyzer (using Gate View), set up the analyzer to view the gated RF signal (see Figure 14-1. and Figure 14-2. for examples of the display):

1. Set the analyzer to the Spectrum Analyzer mode:

   Press **Mode**, **Spectrum Analyzer**, **Mode Preset**.

2. Set the analyzer center frequency, span and reference level:

   Press **FREQ Channel**, **Center Freq**, 40, **MHz**.
   Press **SPAN X Scale**, **Span**, 500, **kHz**.
   Press **AMPTD Y Scale**, **Ref Level**, 10, **dBm**.

3. Set the analyzer bandwidth:

   Press **BW**, **Res BW** (Man), 100, **kHz**.

4. Set the gate source to the rear external trigger input:

   Press **Sweep/Control**, **Gate**, **More**, **Gate Source**, **External 1**.

5. Enable Gate View and Gate:

   Press **Sweep/Control**, **Gate**, **Gate View** (On).
   Press **Gate View Sweep Time**, 10, **ms**.

6. Set the gate delay and gate length so that the gate will open during the middle third of the pulse. For this example, this would result in a Gate Delay of approximately 1.33 ms and a Gate Length of approximately 1.33 ms. Also, check that the gate trigger is set to edge:

   Press **Sweep/Control**, **Gate**, **Gate Delay**, 1.33, **ms**.
   Press **Gate Length**, 1.33, **ms**.
   Press **More**, **Control** (Edge).

Figure 14-1. Gated RF Signal
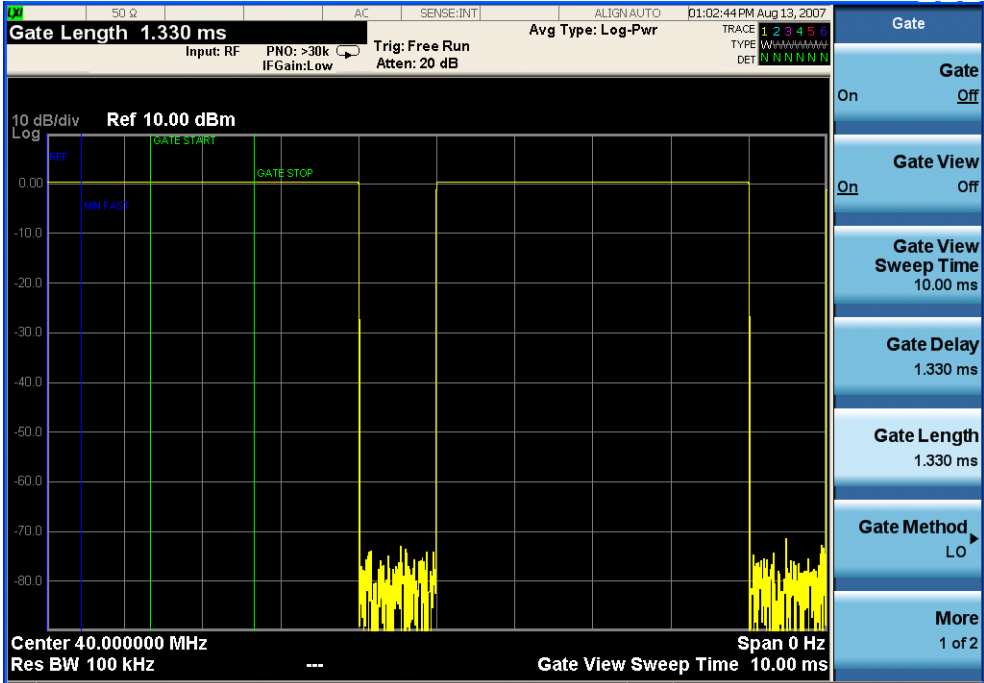
7. Set the RBW to auto, gate view to off, gate method to LO, and gate to on:

Press **Sweep/Control**, **Gate**, **Gate View** (Off).
Press **BW**, **Res BW** (Auto).
Press **Sweep/Control**, **Gate**, **Gate Method**, **LO**.
Press **Gate** (On).

Figure 14-2. Gated RF Signal with Auto RBW
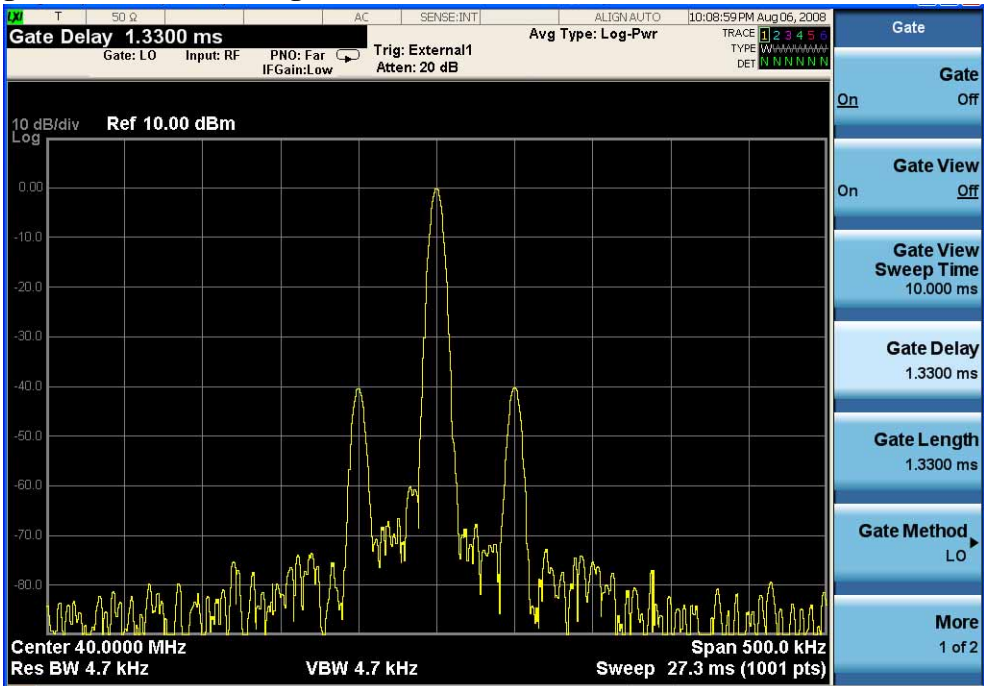
Step 4. If you are using a digitizing oscillascope, set up the oscilloscope to view the trigger, gate and RF signals (see Figure 14-3. for an example of the oscilloscope display):

Table 14-4. Agilent Infiniium Oscilloscope with 3 or more input channels: Instrument Connections

Timebase	1 ms/div
Channel 1	ON, 2 V/div, OFFSET = 2 V, DC coupled, 1 M Ω input, connect to the pulse signal (ESG LF OUTPUT or pulse generator OUTPUT). Adjust channel 1 settings as necessary.
Channel 2	ON, 500 mV/div, OFFSET = 2 V, DC coupled, 1 M Ω input, connect to the signal analyzer TRIGGER 2 OUT connector. Adjust channel 2 settings as needed when gate is active.
Channel 3	ON, 500 mV/div, OFFSET = 0 V, Timebase = 20 ns/div, DC coupled, 50 Ω input, connect to the ESG RF OUTPUT pulsed-RF signal. Adjust channel 3 settings as necessary.
Channel 4	OFF
Trigger	Edge, channel 1, level = 1.5 V, or as needed

Figure 14-3.   Viewing the Gate Timing with an Oscilloscope Channel 1 and 2
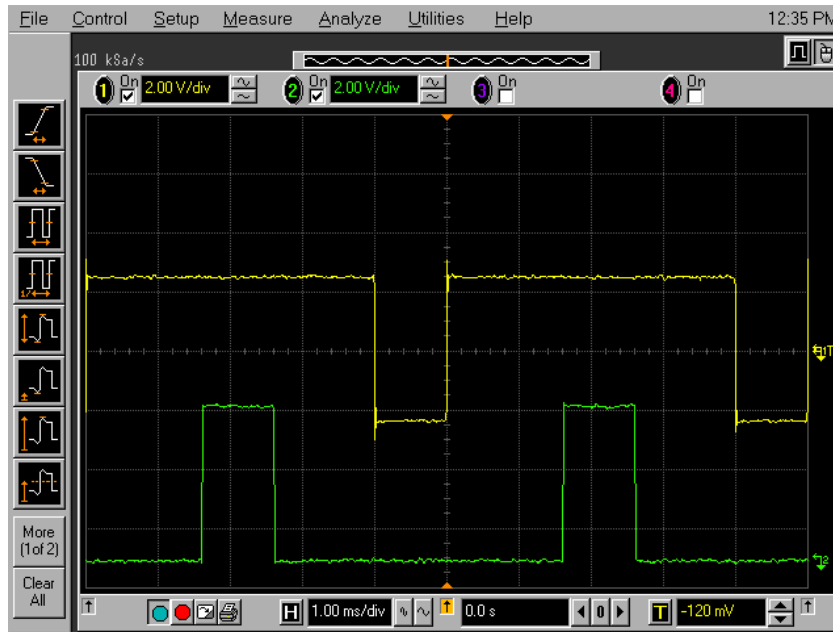
Figure 14-4.   Viewing the Gate Timing with an Oscilloscope Channel 3
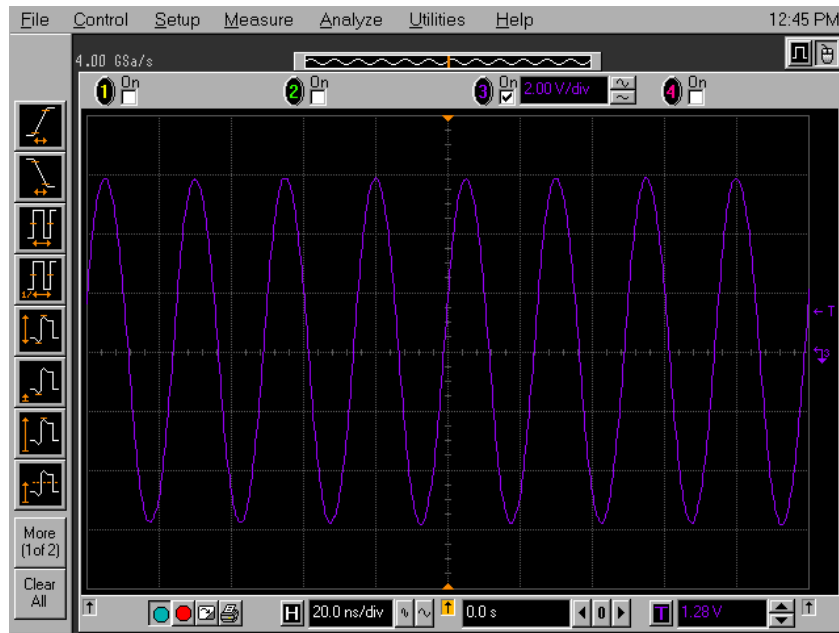
Figure 14-3. Oscilloscope channels:

Channel 1 (top trace) - the trigger signal.

Channel 2 (bottom trace) - the gate signal (gate signal is not active until the gate is on in the spectrum analyzer).

Figure 14-4.Oscilloscope channel:

Channel 3 (right display) - the RF output of the signal generator.

Connecting the Instruments to Make Time-Gated Measurements

Figure 14-5. shows a diagram of the test setup. ESG #1 produces a pulsed FM signal by using an external pulse signal. The external pulse signal is connected to the front of the ESG #1 to the EXT 2 INPUT to control the pulsing. The pulse signal is also used as the trigger signal. The oscilloscope is useful for illustrating timing interactions between the trigger signal and the gate. The Gate View feature of the X-Series signal analyzer could be used in place of the oscilloscope.

Using this measurement setup allows you to view all signal spectra on the spectrum analyzer and all timing signals on the oscilloscope. This setup is helpful when you perform gated measurements on unknown signals. If an oscilloscope is not available, begin by using the Gate View feature to set up the gate parameters and then turn Gate View Off to view the signal spectra, refer to Figure 14-6.

Figure 14-5.   Instrument Connection Diagram with Oscilloscope
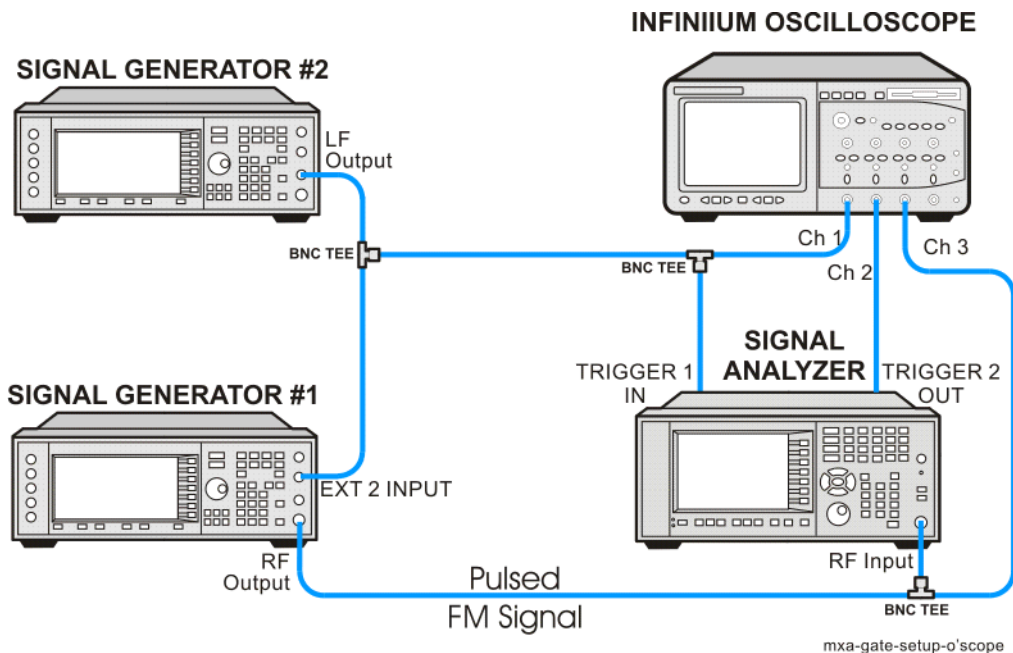
Figure 14-6.   Instrument Connection Diagram without Oscilloscope
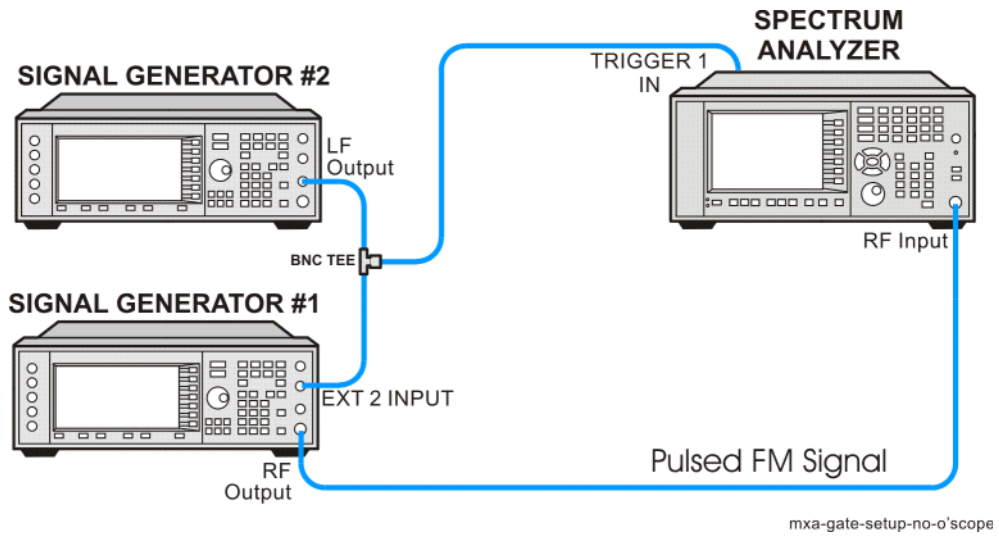
Gated LO Measurement

This procedure utilizes gated LO to gate the FM signal. For concept and theory information about gated LO see "How Time Gating Works" on page 149.

Step 1. Set the analyzer to the Spectrum Analyzer mode:

Press **Mode**, **Spectrum Analyzer**, **Mode Preset**.

Step 2. Set the analyzer center frequency, span and reference level:

Press **FREQ Channel**, **Center Freq**, 40, **MHz**.
Press **SPAN X Scale**, **Span**, 500, **kHz**.
Press **AMPTD Y Scale**, **Ref Level**, 10, **dBm**.

In Figure 14-8., the moving signals are a result of the pulsed signal. Using delta markers with a time readout, notice that the period of the spikes is at 5 ms (the same period as the pulse signal). Using time gating, these signals well be blocked out, leaving the original FM signal.

Step 3. Set the gate source to the rear external trigger input:

Press **Sweep/Control**, **Gate**, **More**, **Gate Source**, **External 1**.

Step 4. Set the gate delay to 2 ms, the gate length to 1 ms, and gate sweep time to 5 ms. Check that the gate trigger is set to edge:

Press **Sweep/Control**, **Gate**, **Gate Delay**, 2, **ms**.
Press **Gate Length**, 1, **ms**.
Press **Gate View Sweep Time**, 5, **ms**.
Press **More**, **Control** (Edge).

Step 5. Use the analyzer gate view display to confirm the gate "on" time is during the RF burst interval (alternatively you could also use the oscilloscope to view the gate settings):

Press **Sweep/Control**, **Gate**, **Gate View** (On).

Figure 14-7.   Viewing the Gate Settings with Gated LO
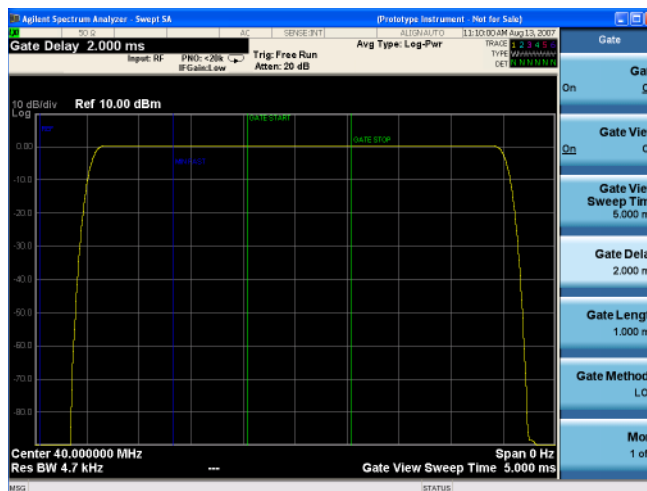
In Figure 14-7. the blue vertical line (the far left line outside of the RF envelope) represents the location equivalent to a zero gate delay.

In Figure 14-7. the vertical green parallel bars represent the gate settings. The first (left) bar (GATE START) is set at the delay time while the second (right) bar (GATE STOP) is set at the gate length, measured from the first bar. The trace of the signal in this time-domain view is the RF envelope. The gate signal is triggered off of the positive edge of the trigger signal.

When positioning the gate, a good starting point is to have it extend from 20% to 80% of the way through the pulse.

While gate view mode is on, move the gate delay, length and polarity around. Notice the changes in the vertical gate bars while making your changes. Set the gate delay, length and polarity back to the step 3 settings.

NOTE   The analyzer time gate triggering mode uses positive edge, negative edge, and level triggering.

Step 6. Turn the gate view off (see Figure 14-8.):

Press **Sweep/Control**, **Gate**, **Gate View** (Off).

Figure 14-8.   Pulsed-RF FM Signal
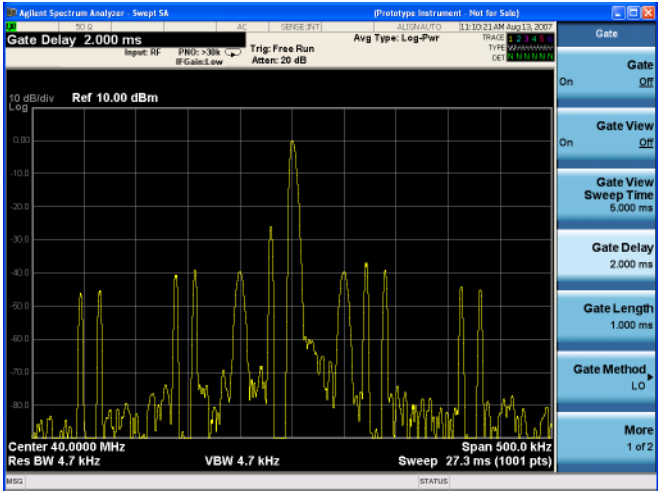
Step 7. Enable the gate settings (see Figure 14-9.):

Press **Gate** (On).

Figure 14-9.   Pulsed and Gated FM Signal
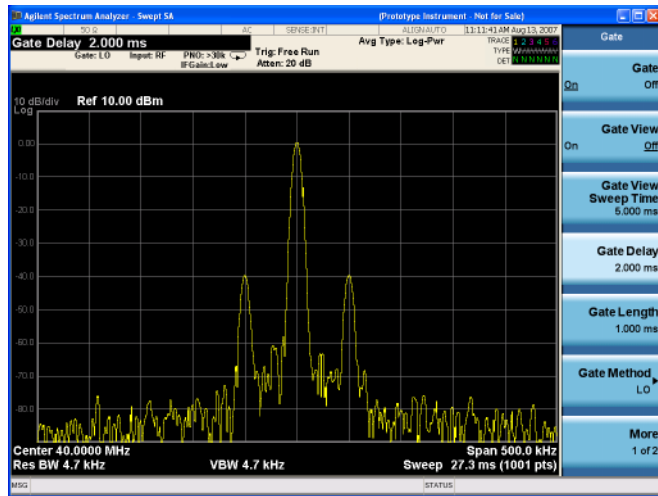
Step 8. Turn off the pulse modulation on ESG #1 by pressing **Pulse**, **Pulse** so that Off is selected.

Notice that the gated spectrum is much cleaner than the ungated spectrum (as seen in Figure 14-8.). The spectrum you see with the gate on is the same as a frequency modulated signal without being pulsed. The displayed spectrum does not change and in both cases, you can see the two low-level modulation sidebands caused by the narrow-band FM.

Gated Video Measurement

This procedure utilizes gated video to gate the FM signal. For concept and theory information about gated video see "How Time Gating Works" on page 149.

Step 1. Set the analyzer to the Spectrum Analyzer mode:

Press **Mode**, **Spectrum Analyzer**, **Mode Preset**.

Step 2. Set the analyzer center frequency, span and reference level:

Press **FREQ Channel**, **Center Freq**, 40, **MHz**.
Press **SPAN X Scale**, **Span**, 500, **kHz**.
Press **AMPTD Y Scale**, **Ref Level**, 10, **dBm**.

Step 3. Set analyzer points to 401 and sweep time to 2000 ms:

Press **Sweep/Control**, **Points**, 401, **Enter**.
Press **Sweep Time**, 2000, **ms**.

For gated video, the calculated sweep time should be set to at least $(\# \text{ sweep points} - 1) \times \text{PRI (pulse repetition interval)}$ to ensure that the gate is on at least once during each of the 401 sweep points. In this example, the PRI is 5 ms, so you should set the sweep time to 401 minus 1 times 5 ms, or 2 s. If the sweep time is set too fast, some trace points may show values of zero power or other incorrect low readings. If the trace seems incomplete or erratic, try a longer sweep time.

NOTE   **Good practices for determining the minimum sweep time for gated video:**

In the event that the signal is not noisy, the sweep time can be set to less than $(\# \text{ sweep points} - 1) \times \text{PRI (pulse repetition interval)}$ (as calculated above). Instead of using PRI in the previous sweep time calculation, we can use the "gate off time" where sweep time equals $(\# \text{ sweep points} - 1) \times \text{gate off time}$. (Gate off time is defined as $\text{PRI} - \text{GL}$, where GL = Gate Length.) In our example we could use a sweep time of 400 points times 1 ms or 400 ms $- (401 - 1) \times (5\text{ms} - 4\text{ms}) = 400\text{ms}$. Increase the video bandwidth to improve the probability of capturing the pulse using "gate off time". If trace points are still showing values of zero power, increase the sweep time by small increments until there are no more dropouts.

Step 4. Set the Gate source to the external trigger input on the rear panel:

Press **Sweep/Control**, **Gate**, **More**, **Gate Source**, **External 1**.

Figure 14-10. Viewing the Pulsed-RF FM Signal (without gating)
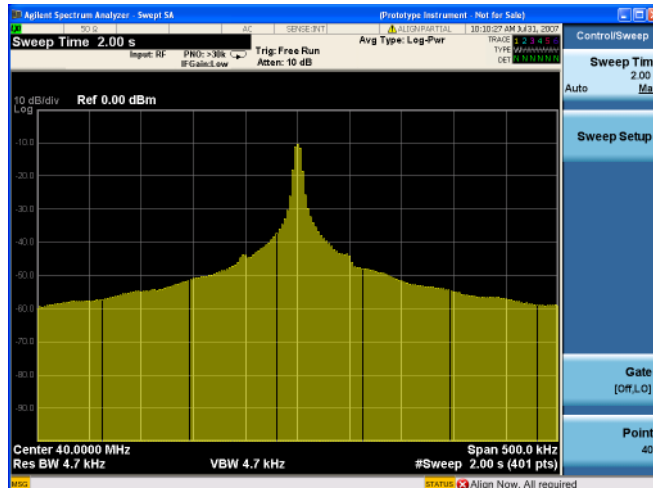
Step 5. Set the gate delay to 2 ms and the gate length to 1 ms. Check that the gate control is set to edge:

Press **Sweep/Control**, **Gate**, **More**, **Control** (Edge).
Press **More**, **Gate Delay**, 2, **ms**.
Press **Gate Length**, 1, **ms**.

Step 6. Turn the gate on:

Press **Sweep/Control**, **Gate**, **Gate Method**, **Video**
Press **Gate** (On).

Figure 14-11. Viewing the FM Signal of a Pulsed RF Signal using Gated Video
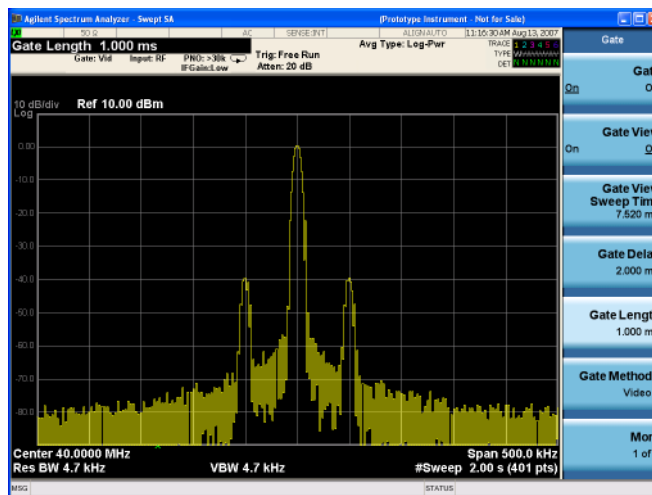
Step 7. Notice that the gated spectrum is much cleaner than the ungated spectrum (as seen in Figure 14-10.). The spectrum you see is the same as a frequency modulated signal without being pulsed. To prove this, turn off the pulse modulation on ESG #1 by pressing **Pulse**, **Pulse** so that Off is selected. The displayed spectrum does not change.

Step 8. If you have used an oscilloscope, check the oscilloscope display and ensure that the gate is positioned under the pulse. The gate should be set so that it is on somewhere between 20% to 80% of the pulse. If necessary, adjust gate length and gate delay. Figure 14-12. shows the oscilloscope display when the gate is positioned correctly (the bottom trace).

Figure 14-12. The Oscilloscope Display
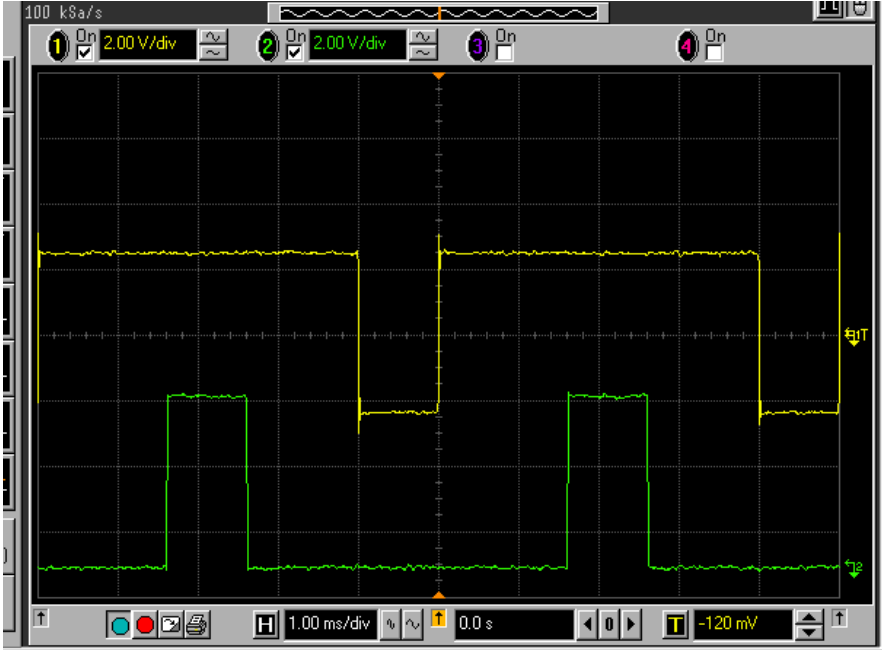
Gated FFT Measurement

This procedure utilizes gated FFT to gate the FM signal. For concept and theory information about gated FFT see "How Time Gating Works" on page 149.

Step 1. Set the analyzer to the Spectrum Analyzer mode:

Press **Mode**, **Spectrum Analyzer**, **Mode Preset**.

Step 2. Set the analyzer center frequency, span and reference level:

Press **FREQ Channel**, **Center Freq**, 40, **MHz**.
Press **SPAN X Scale**, **Span**, 500, **kHz**.
Press **AMPTD Y Scale**, **Ref Level**, 10, **dBm**.

Step 3. Set the Gate source to the external rear trigger input:

Press **Sweep/Control**, **Gate**, **More**, **Gate Source**, **External 1**.

Step 4. Set the Gate Method to FFT and Gate to On:

Press **Sweep/Control**, **Gate**, **Gate Method**, **FFT**
Press **Gate** (On).

Step 5. Select the minimum resolution bandwidth required:

Press **BW**, **Res BW** (Auto).

Figure 14-13. Viewing the Gated FFT Measurement Results
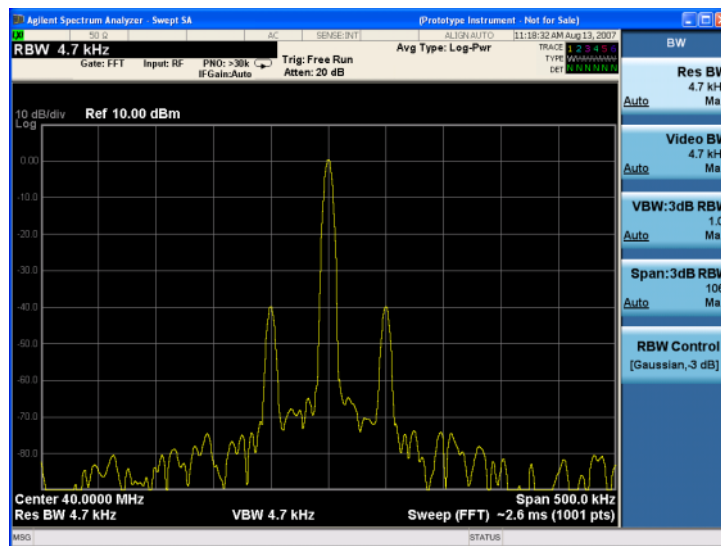
The duration of the analysis required is determined by the RBW. Divide 1.83 by 4 ms to calculate the minimum RBW. The pulse width in our case is 4 ms so we need a minimum RBW of 458 Hz. In this case because the RBW is so narrow let the analyzer choose the RBW for the current analyzer settings (span). Check that the RBW is greater than 458 Hz.

With the above analyzer settings, the RBW should be 4.7 kHz. Note that the measurement speed is faster than the gated LO example. Typically gated FFT is faster than gated LO for spans less than 10 MHz.

Vary the RBW settings and note the signal changes shape as the RBW transitions from 1 kHz to 300 Hz.

NOTE   If the trigger event needs to be delayed use the **Trig Delay** function under the **Trigger** menu. It is recommended to apply some small amount of trigger delay to allow time for the device under test to settle.

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15 HSDPA and HSUPA Concepts

HSDPA Concepts

What is HSDPA?

High Speed Downlink Packet Access (HSDPA) is a digital packet communications format that supports high speed data transmission within the existing W-CDMA communications system. Appropriate uses for HSDPA are DL data bit streams like those employed for Internet browsing, video, and GPS mapping data. HSDPA physical layer code channels are defined in 3GPP TS.25.211-214 v.5xx.

HSDPA is a packet-based data service that operates inside a W-CDMA downlink with data transmission up to 8-10 Mbps (and 20 Mbps for MIMO systems) over a 5MHz bandwidth in WCDMA downlink. HSDPA implementations as defined by 3GPP include Adaptive Modulation and Coding (AMC), Multiple-Input Multiple-Output (MIMO), Hybrid Automatic Rate reQuest (HARQ), and fast cell search.

Protocol Structure

The protocol structure of the HSDPA system is the same as the W-CDMA protocol structure as shown in Figure 15-1. HSDPA employs existing W-CDMA logical channels, but uses different transport and physical layer channels. Figure 15-1 shows the three bottom W-CDMA layers, and the corresponding HSDPA channels.

Figure 15-1   **W-CDMA Protocol Structure w/ HSDPA Channel Overlay**
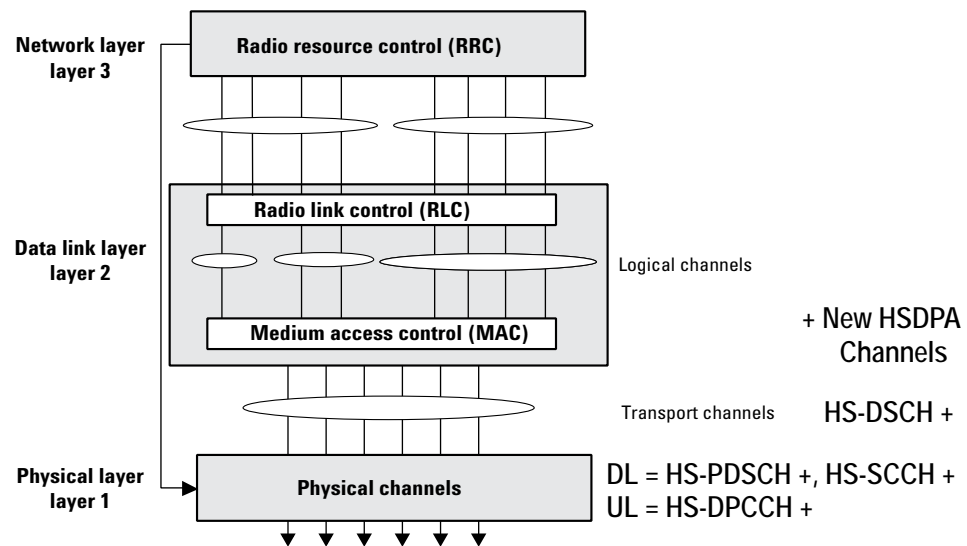
HSDPA Logical, Transport, and Physical Channels

HSDPA cooperates with existing W-CDMA transport channels to support sharing

physical resources between multiple services. Each service, such as data, fax, voice, or signaling, is routed into different transport channels by the upper signaling layers. These services may have different data rates and error control mechanisms. The transport channels are then multiplexed as required prior to transmission via one or more physical channels. High data rate services or a combination of lower rate transport channels may be multiplexed into several physical channels. This flexibility allows numerous transport channels (services) of varying data rates to be efficiently allocated to physical channels. By multiplexing these transport channels efficiently, system capacity is optimized. For example, if the aggregate data rate of three transport channels exceeds the maximum of a single physical channel, then the data can be routed to two lower rate physical channels that closely match the total required data rate. Transport channels include the Broadcast Channel (BCH), the Paging Channel (PCH), the Forward Access Channel (FACH), the Dedicated Channel (DCH), the HSDPA High-Speed Downlink Shared Channel (HS-DSCH, which corresponds to the HS-PDSCH) and the Random Access Channel (RACH). [7]

HSDPA also cooperates with W-CDMA DL physical channels. The most important DL physical channels are the Common Pilot Channel (CPICH), the Primary Common Control Physical Channel (P-CCPCH), the Secondary Common Control Physical Channel (S-CCPCH), the Dedicated Physical Data and Control Channels (DPDCH/DPCCH), the HSDPA High-Speed Physical Downlink Shared Channel (HS-PDSCH), and the HSDPA Shared Control Channel (HS-SCCH). The UL consists of a Physical Random Access Channel (PRACH), a Physical Common Packet Channel (PCPCH), Dedicated Physical Data and Control Channels (DPDCH/DPCCH), and the HSDPA Dedicated UL Physical Control Channel (HS-DPCCH). The W-CDMA channels above are described in the following sections.

Figure 15-2   HSDPA Logical, Transport, and Physical Channel Mapping
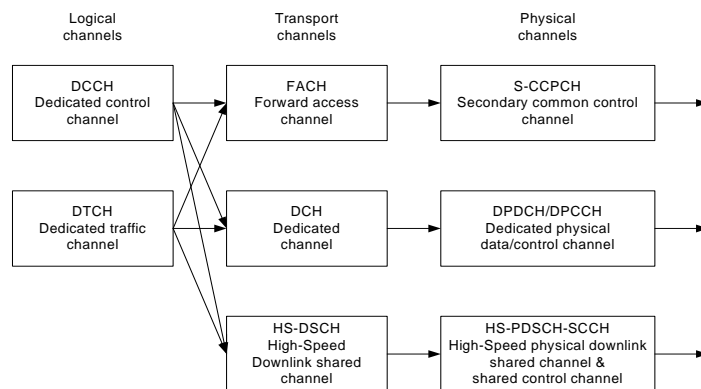
Figure 15-2 on page 99 shows an example of channel mapping for the DL. When a UE is in idle mode (not in High-Speed mode), the BTS sends dedicated signaling information from the DCCH logical channel through the FACH transport channel. This maps the information onto the S-CCPCH physical channel for transmission to a UE. When the UE is in the High-Speed connection mode, the same signaling information is routed through the HS-DSCH transport channel. This maps the information onto the HS-SCCH physical channel for transmission to the UE.

Downlink Physical Channels

High-Speed Shared Control Channel (HS-SCCH)

The HS-SCCH is a fixed rate (60 kbps, SF=128) downlink physical channel used to carry downlink signalling related to HS-DSCH transmission. Figure 15-3 illustrates the sub-frame structure of the HS-SCCH.

Figure 15-3   **Subframe Structure of HS-SCCH**

Data
N_{data1} bits

T_{slot} = 2560 chips, 40 bits

| Slot #0 | Slot#1 | Slot #2 |

1 HS-DSCH subframe: T_f= 2 ms
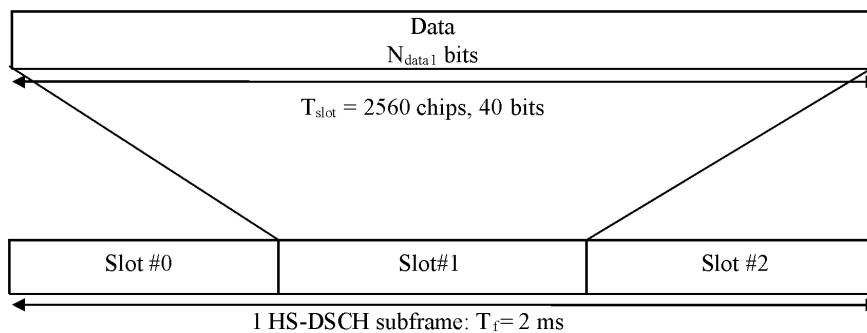
Slot #0 carries modulation information of HS-PDSCH, such as Channelization Code Set and Modulation Scheme.

Slots #1 and #2 carry channel-coding information of HS-DSCH shown below. Data contained in Slot #0,#1,#2 is "covered" with UE identity.

The following information is transmitted by means of the HS-SCCH physical channel:

- Channelization-code-set information (7 bits)

- Modulation scheme information (1 bit)

- Transport-block size information (6 bits)

- Hybrid-ARQ process information (3 bits)

- Redundancy and constellation version (3 bits)

- New data indicator (1 bit)

- UE identity (16 bits)

Figure 15-4 on page 102 shows the HS-SCCH channel coding.

Figure 15-4 **HS-SCCH Channel Coding**
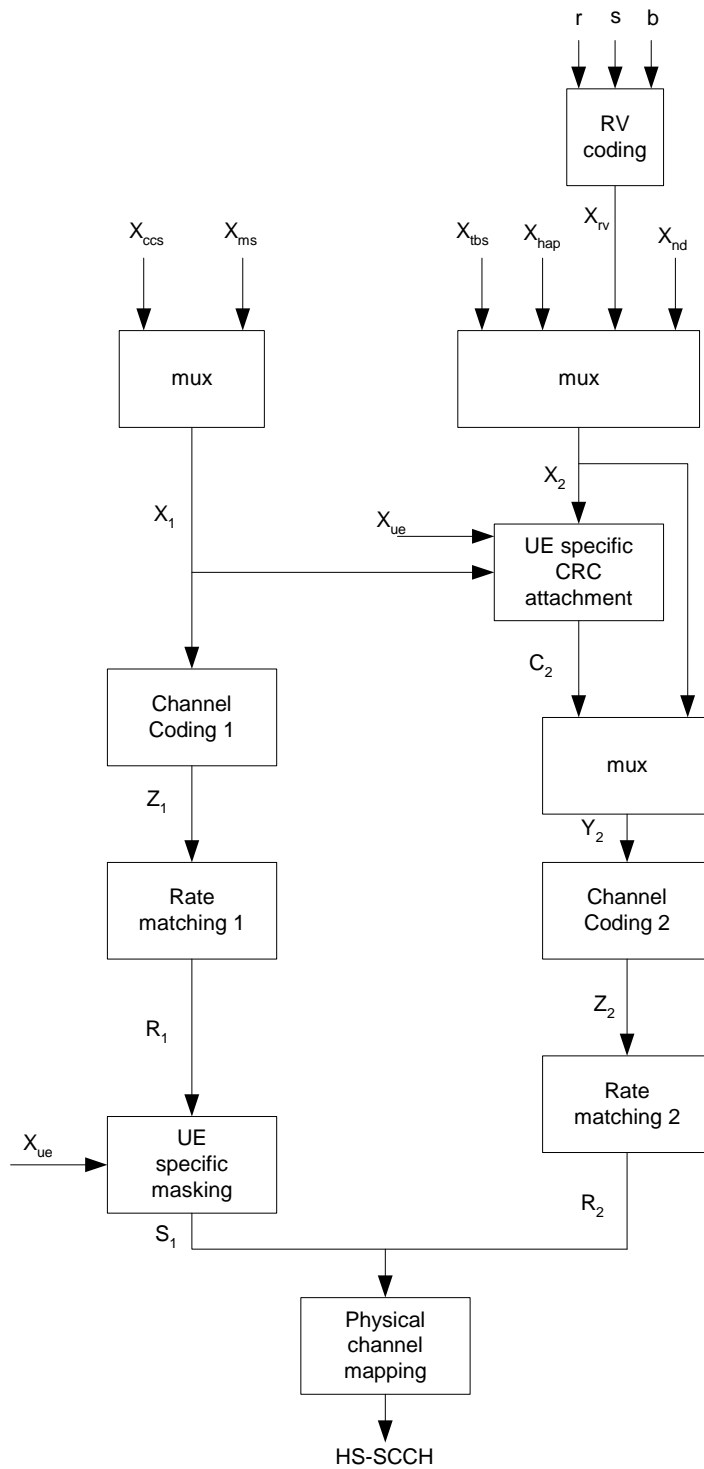
High-Speed Physical Downlink Shared Channel (HS-PDSCH)

The High Speed Physical Downlink Shared Channel (HS- PDSCH) is used to carry the High Speed Downlink Shared Channel (HS-DSCH).

An HS-PDSCH corresponds to one channelization code of fixed spreading factor SF=16 from the set of channelization codes reserved for HS-DSCH transmission. Multi-code transmission is allowed, which translates to UE being assigned multiple channelization codes in the same HS-PDSCH subframe, depending on its UE capability. Table 15-6 shows the HS-DSCH data fields.

Figure 15-5   Subframe Structure for HS-PDSCH

$$\text{Data}$$
$$N_{data1}\text{ bits}$$

$$T_{slot} = 2560\text{ chips, }M*10*2^{k}\text{ bits (k=4)}$$

| Slot #0 | Slot#1 | Slot #2 |

$$1\text{ HS-PDSCH subframe: }T_f = 2\text{ ms}$$
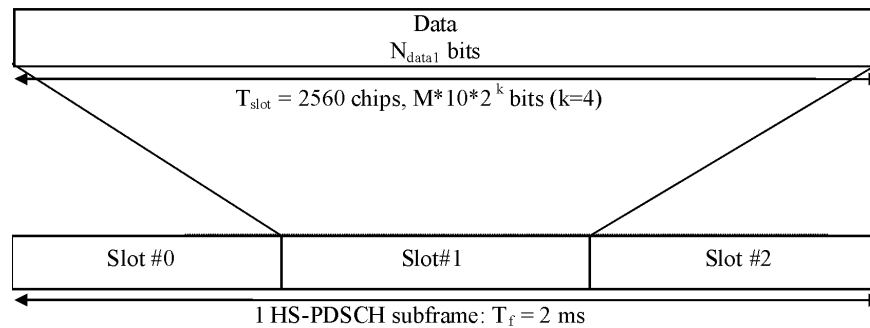
An HS-PDSCH may use QPSK or 16QAM modulation symbols. In Figure 15-5 above, M is the number of bits per modulation symbols i.e. M=2 for QPSK and M=4 for 16QAM

The subframe and slot structure of HS-PDSCH is shown in Figure 15-5. An HS-PDSCH may use QPSK or 16QAM modulation symbols. In Figure 15-5, M is the number of bits per modulation symbols i.e. M=2 for QPSK and M=4 for 16QAM. The slot formats are shown in Table 15-6 on page 103.

Figure 15-6   HS-DSCH Fields

Slot Format #i	Channel Bit Rate (kbps)	Channel Symbol rate	SF	Bits per HS-DSCH Subframe	Bits/Slot	Ndata
0 (QPSK)	480	240	16	960	320	320
1 (16QAM)	960	240	16	1920	640	640

Downlink HS-PDSCH Coding and Air Interface

Figure 15-7 depicts how the downlink HS-DSCH transport channel is coded into physical HS-PDSCH channel(s). The output of "Physical channel segmentation" can be multiple code channels, in this example, there are 2. In this manner one HS-DSCH transport channel can be mapped to two or more physical HS-PDSCH channels to support higher data rates.

Figure 15-7   Downlink HS-PDSCH Coding, Spreading, and Scrambling
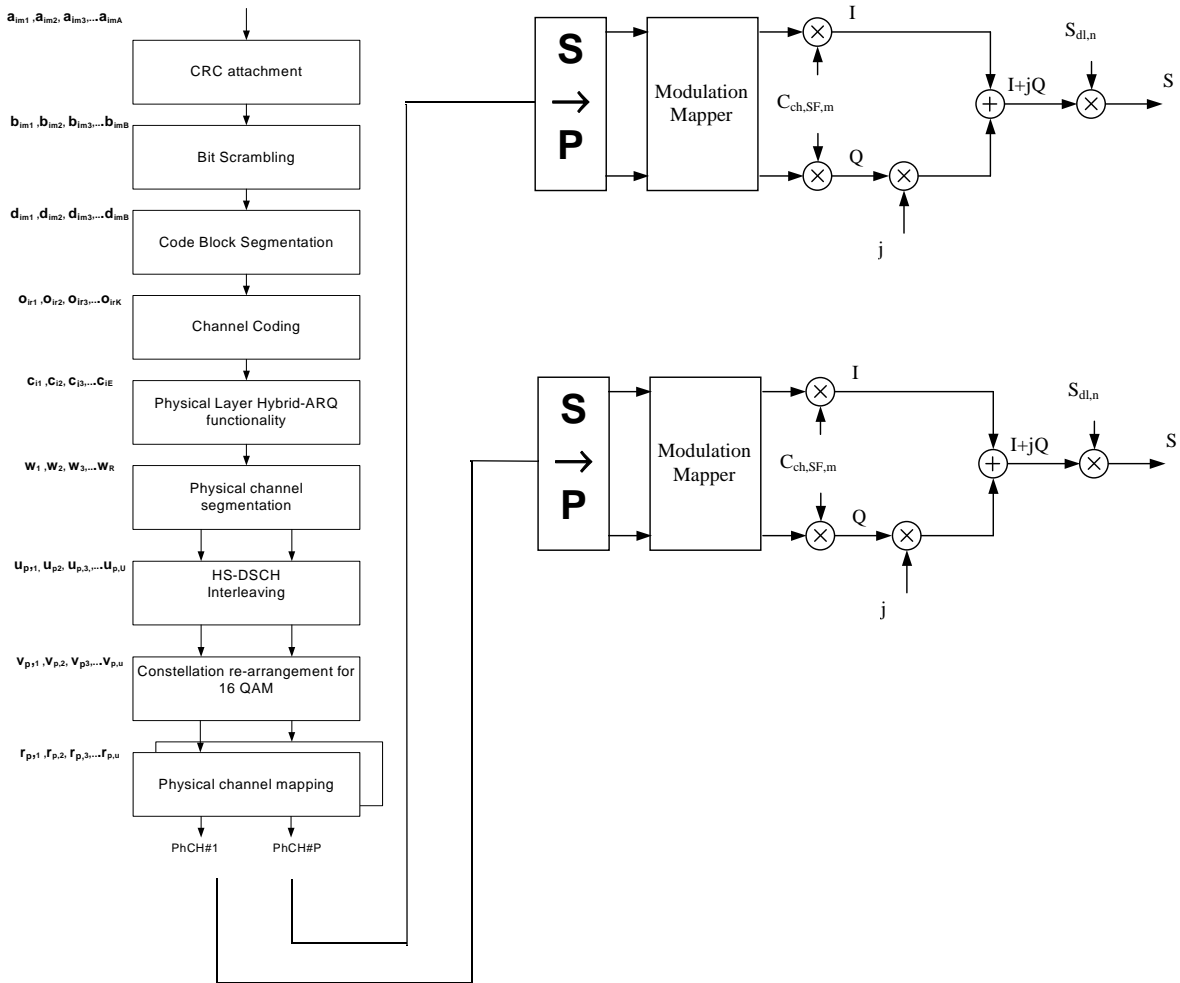
HSDPA Test Model 5

The Agilent X-Series provides complete HSDPA measurements to make the same suite of tests as for W-CDMA, but a new Test Model has been added to allow HSDPA signals to be analyzed. 3GPP specifications require that Test Model 5 be used for qualification of base station equipment, so it is provided in the **Meas Setup, Symbol Boundary** menus for Modulation Accuracy (Composite EVM) and Code Domain Power measurements, along with the four previous W-CDMA test models.

3GPP Test Model 5 specifications include two new code channels; the High-Speed Physical Downlink Shared Channel (HS-PDSCH) and the High-Speed Shared Control Channel for HS-DSCH (HS-SCCH).

Figure 15-8 **HSDPA Test Model 5 Code Channels**

Code Channel	Symbol Encoding	OVSF Spread Factor
HS-PDSCH	16QAM	16 (640 symbols/slot)
HS-SCCH	QPSK	128

These code channels are described in detail in the section, "Downlink Physical Channels" on page 100.

Uplink Physical Channel

High-Speed Dedicated Physical Control Channel (HS-DPCCH)

The HS-DPCCH carries uplink feedback signalling related to downlink HS-DSCH transmission. The HS-DSCH-related feedback signalling consists of Hybrid-ARQ Acknowledgement (HARQ-ACK) and Channel-Quality Indication (CQI). Each sub frame of length 2 ms (3*2560 chips) consists of 3 slots, each of length 2560 chips. The HARQ-ACK is carried in the first slot of the HS-DPCCH sub-frame. The CQI is carried in the second and third slot of an HS-DPCCH sub-frame. There is at most one HS-DPCCH on each radio link. The HS-DPCCH can only exist together with an uplink DPCCH.

Figure 15-9   **Subframe Structure for HS-DPCCH**

T_{slot} = 2560 chips $2 \times T_{slot}$ = 5120 chips

HARQ-ACK	CQI

One HS-DPCCH subframe (2 ms)

Subframe #0	Subframe #i	Subframe #4

One radio frame T_f = 10 ms
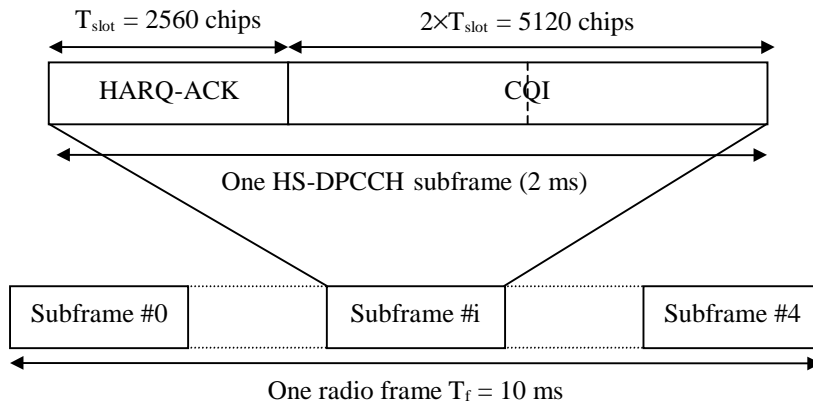
Figure 15-10   **HS-DPCCH Fields**

Slot Format #i	Channel Bit Rate (ksps)	Channel Symbol Rate (ksps)	SF	Bits per Subframe	Bits per Slot	Xmitted Slots per Frame
0	15	15	256	30	10	3

Uplink HS-DPCCH Coding and Air Interface

The input summation block, spreading, and scrambling used on the UL HS-DPCCH is shown in Figure 15-11. The diagram shows an example of the coding and air interface for a UL HS-DPCCH and multiple DPDCH channels. In the case of only one DPDCH, the W-CDMA coding shown in Figure 15-11 is employed. The summing scheme shown below is also used for non-HS coding when more than one DPDCH is employed.

The channelization scheme used for the summation block is shown in Table 15-1 on page 108.

Figure 15-11   **Uplink DPDCH/HS-DPCCH Coding, Spreading, and Scrambling.**
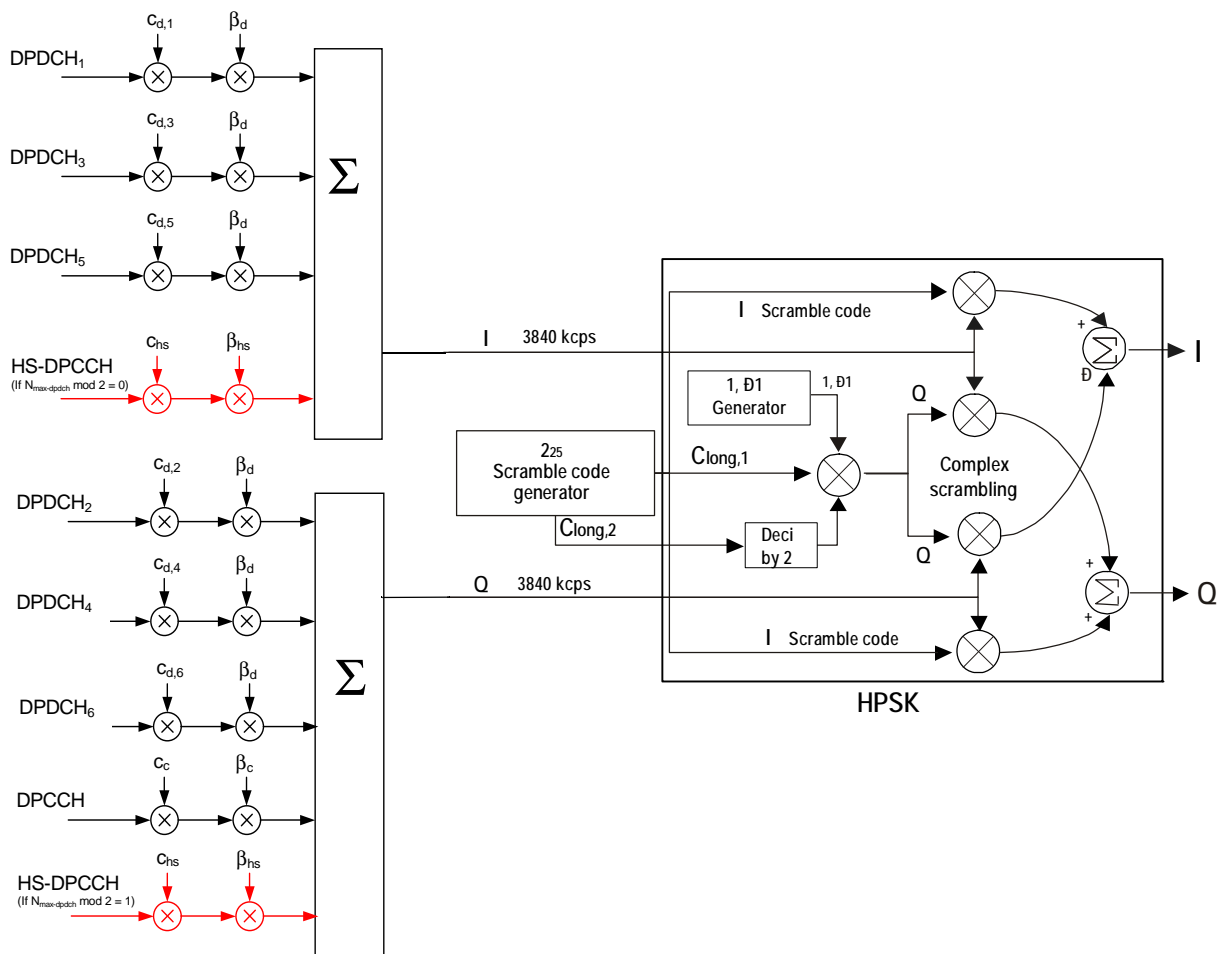
Table 15-1   Channelization Code of HS-DPCCH

$N_{max\text{-}dpdch}$	Channelization Code Cch
0	$C_{ch,256,33}$
1	$C_{ch,256,64}$
2,4,6	$C_{ch,256,1}$
3,5	$C_{ch,256,32}$

In order to balance total power on I and Q axes, HS-DPCCH's channelization code varies depending on DPDCH channel's activity status. There are two possible HS-DPCCH positions on the summation block. If the number of DPDCH is even, HS-DPCCH is included in I-summation. If the number of DPDCH is odd, HS-DPCCH is included in Q-summation. Table 15-1 shows that HS-DPCCH's code number varies by the number of DPDCH. For example, if there are three DPDCH channels, the HS-DPCCH code number is 32, and since "three" is an odd number of DPDCH channels, the HS-DPCCH is included in Q-axis summation.

HSDPA Physical Channel Timing

Figure 15-12 shows the relationship between the HS-SCCH and the HS-PDSCH physical channels in the DL.

Figure 15-12   HS-SCCH/HS-PDSCH Timing (Downlink)
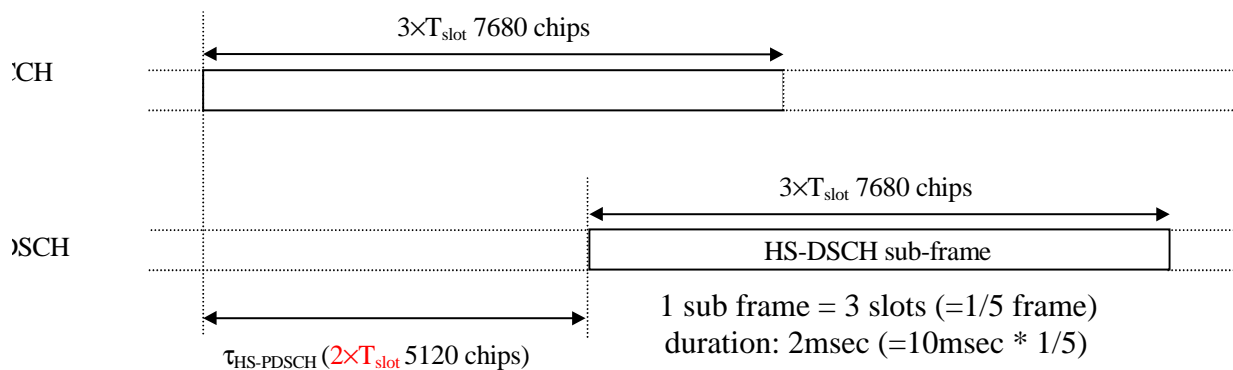
The HS-PDSCH starts τHS-PDSCH = 2' Tslot = 5120 chips after the start of the HS-SCCH.

Figure 15-13 shows a diagram of the radio frame timing relationships between the UL and DL physical channels.

Figure 15-13   Radio Frame Timing of UL and DL Physical Channels
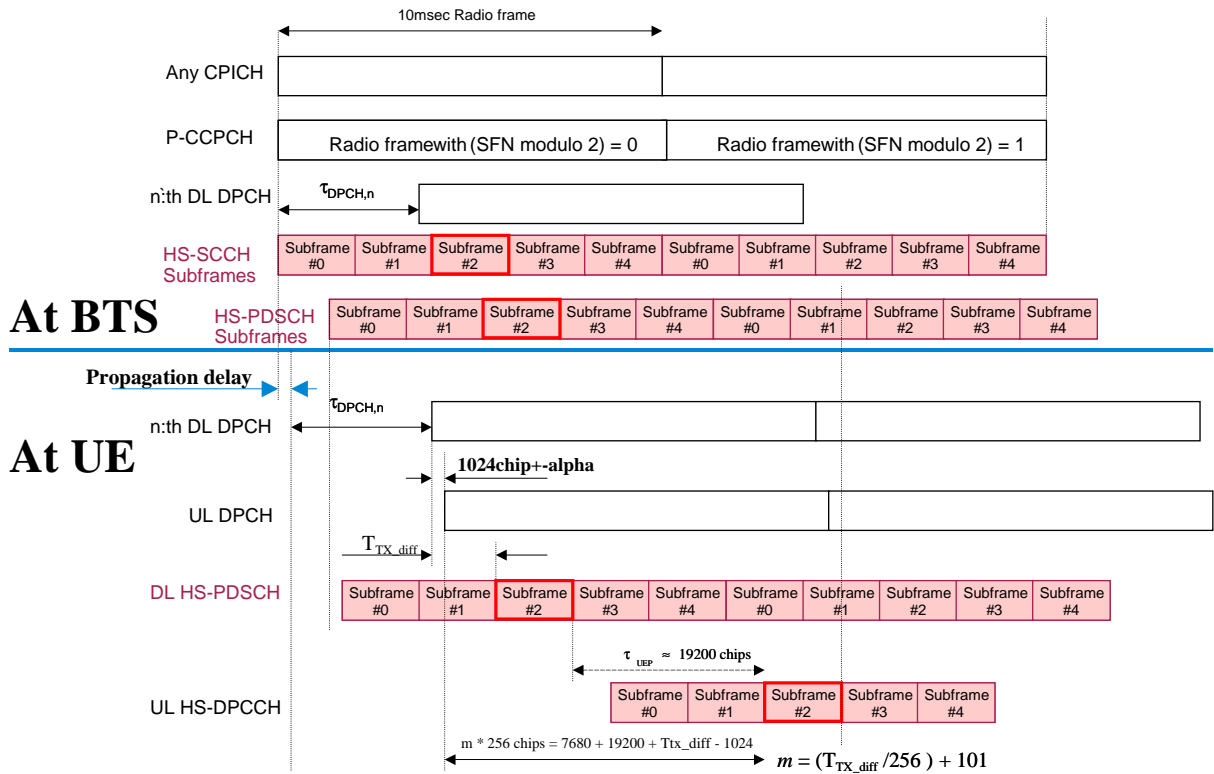
Transport Format Detection

HSDPA uses the W-CDMA Transport Format Combination Set (TFCS), to communicate from the network to the UE at the time of connection setup. The TFCS includes all of the allowable Transport Formats (TF) and the associated data capacity for each of the channels that can be present in the link, and all of the allowable Transport Format Combinations (TFC) for the link. The Network's Radio Resource Control (RRC) entity provides this information to its lower layers. The UE's RRC entity does the same for its lower layers upon receiving the TFCS from the network. Once this information is shared between the two, the transmitter can use it, along with the demands for transmission capacity from higher layers, to decide which channels shall be present and how each channel will be arranged in the radio frame. Likewise the receiver can use it to determine which channels are present and how to recover each channel that is present.

HSDPA also uses the same two W-CDMA methods to make this determination. The first of these is the inclusion of a Transport Format Combination Indicator (TFCI) in each radio frame. The second is Blind Transport Format Detection (BTFD). When TFCI is used, the transmitting side determines which Transport Format Combination it will use. It then includes the TFCI, which is an index to the list of allowable combinations in the TFCS, in the control portion of the DPCH. The receiver always knows how to recover the TFCI, which it then uses to determine which channels to try to recover and how to decode each one. When BTFD is used, the receiver must try every allowable TFC in the TFCS to determine which one results in the least errors.

Modulation Scheme Detection

The DL HS-PDSCH may be modulated using either QPSK or 16QAM. MS (UE) gets the modulation scheme in advance of the actual modulated signal from information encoded into the HS-SCCH. The modulation scheme can change dynamically as often as every subframe, or every 3 slots.

HSDPA Measurement Concepts

High speed downlink packet access (HSDPA) is a new packet-based service in the Third Generation Partnership Project (3GPP) Wideband-Code Division Multiple Access (W-CDMA) radio format. Designed to provide higher data throughput on the downlink, it was first introduced in Release 5 of the 3GPP specifications. HSDPA employs adaptive modulation and coding to continually reconfigure the downlink, optimizing data throughput for each user depending on the instantaneous quality of the link. The new service is backwards compatible with 3GPP Release 99 and can be used in conjunction with other services to the same user equipment (UE). Voice and data applications developed for W-CDMA Release 99 can still be run on the upgraded Release 5 networks, and the same radio channel will support W-CDMA and HSDPA services simultaneously.

The changes that HSDPA introduces have test implications in many different areas, including the radio frequency (RF). New UE transmitter and receiver characteristic requirements and a whole new section for UE HSDPA performance requirements have been added to the Release 5 and Release 6 RF conformance test specifications.

Why Test HSPDPA User Equipment?

Although HSDPA is primarily a baseband or signaling extension to W-CDMA, many aspects of the new service require specialized testing.

The main aspects of HSDPA technology that have implications for physical layer testing of the UE are the following:

- The new uplink high speed dedicated physical control channel (HS-DPCCH) increases the peak-to-average power ratio (PAR).

- The uplink HS-DPCCH is not usually transmitted continuously and can be offset in time from the dedicated physical control channel (DPCCH).

- The new 16QAM format in the downlink high speed physical data shared

channel (HS-PDSCH) has less margin for UE receiver impairments than does QPSK.

- Decoding the downlink high speed data shared channel (HS-DSCH) involves complex new functionality.

- Accurate channel quality reporting is crucial to overall system performance.

- Without correct detection of the high speed shared control channel (HS-SCCH) downlink control information, HSDPA communication is not possible.

Each of these areas of change and the implications for testing are next discussed briefly.

HS-DPCCH increases uplink peak-to-average power ratio (PAR)

The biggest change on the uplink is the addition of the high speed dedicated physical control channel (HS-DPCCH).

The standard Release 99 W-CDMA uplink signal, which consists of the dedicated physical data channel (DPDCH) and the DPCCH, can have a peak-to-average power ratio (PAR) at 0.1% from about 3.1 dB to about 3.6 dB, depending on the signal configuration. The new code channel (HS-DPCCH) can add up to ~1 dB to the PAR (at 0.1%) of the uplink signal.

Because the HS-DPCCH is not usually transmitted continuously, the PAR increases only when the acknowledgement/negative acknowledgement (ACK/NACK) or the channel quality indicator (CQI) fields are transmitted. The exact increase in the PAR depends on the beta factors ßc, ßd, and ßhs, which correspond to the relative power levels of the uplink DPCCH, DPDCH, and HS-DPCCH.

A higher PAR can increase the distortion generated by the transmitter, and particularly by the power amplifier, resulting in higher out-of-channel interference and poorer modulation quality. So that Release 99 power amplifiers will work correctly with this higher PAR signal, the maximum output power requirement is reduced when the HS-DPCCH is on.

The following figure illustrates how PAR increases when the ACK/NACK or the CQI fields in the HS-DPCCH are transmitted, and how the maximum composite average output power is reduced to compensate for this increase.

Figure 15-14   **HS-DPCCH Increases Uplink Peak-to-Average Power Ratio (PAR)**
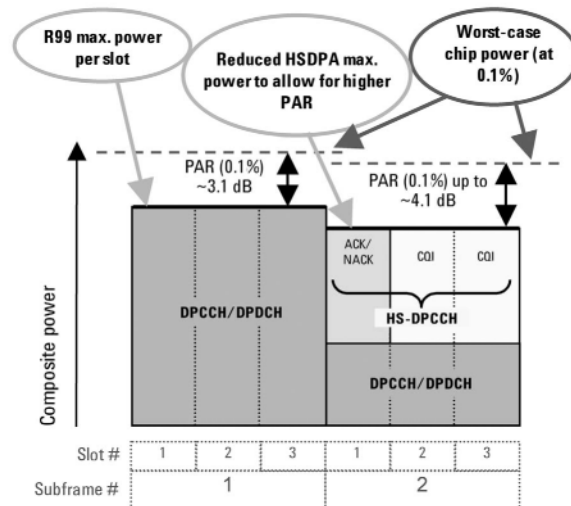
The HS-DPCCH is not usually transmitted continuously and can be offset in time from the DPCCH. Turning the HS-DPCCH on and off can cause power steps of up to 7 dB, depending on the beta factors. The HS-DPCCH is a shared channel and therefore is fixed in time relative to the common pilot channel (CPICH). The DPDCH and DPCCH, however, can be shifted in time in 0.1 slot increments. In the generic example of power versus time shown below, observe that the HS-DPCCH is not aligned in time with these other channels. Additionally, the CQI relative power (CQI) differs from the ACK/NACK relative power (ACK or NACK). So that the accuracy of the power steps can be verified in such cases, a new test of the power-versus-time mask has been added to the specifications.

Figure 15-15   **Transmit Power Template During HS-DPCCH Transmission**
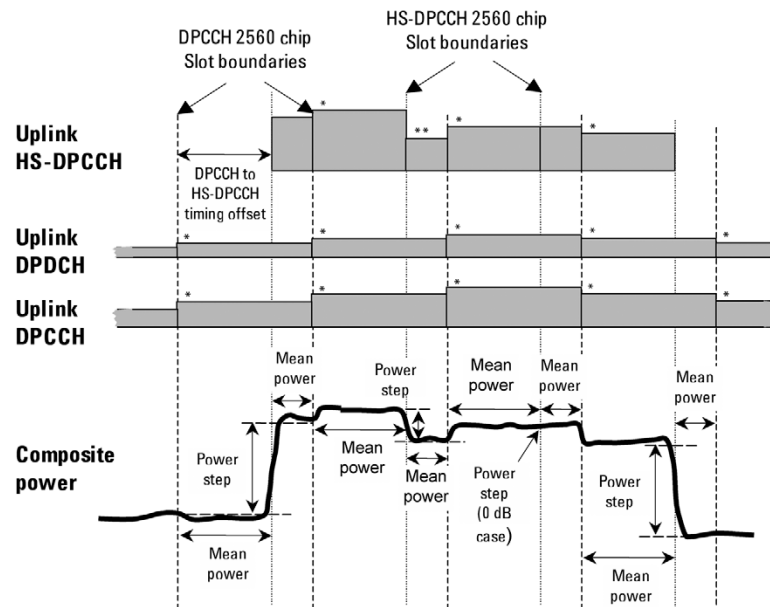
* = step due to inner loop power control
** = step due to CQI transmission

If the HS-DPCCH is not time-aligned with the DPCCH/DPDCH, the 7 dB power
step may occur during transmission of the DPCCH/DPDCH slot. Such an
occurrence introduces the potential for phase transients or other distortions during
the slot transmission, which then degrade the signal quality and impact the ability
of the Node B (base station) to demodulate the DPCCH/DPDCH when the
HS-DPCCH is transmitted. New modulation accuracy requirements being
developed by the 3GPP could address this issue.

Before the UE can decode HSDPA downlink traffic data in the HS-DSCH, it must
first recognize the control information sent by the BTS and carried by the
downlink high speed shared control channel (HS-SCCH). In other words, if the UE
cannot detect the HS-SCCH control information, it will not be able to decode the
payload data on the HS-PDSCH and data throughput will cease. Verifying the
performance of HS-SCCH detection is, therefore, an important test. For this
reason, an HS-SCCH detection test has been added to the specifications.

HSDPA UE RF Conformance Tests

To address the challenges introduced by HSDPA, a number of HSDPA-related tests have been added to the UE RF conformance tests (3GPP TS 34.121) in Release 5 and Release 6.Note that there are five new transmitter tests required in 34.121 Section 5:

- Maximum Output Power With HS-DPCCH (34.121 5.2A)

- Transmit On/Off Power – HS-DPCCH (34.121 5.7A)

- SEM (34.121 5.9A)

- ACLR (34.121 5.10A)

- EVM (34.121 5.13.1A)

One new test of receiver characteristics is required in 34.121 Section 6:

- Maximum Input Level for HS-PDSCH Reception Using 16QAM (34.121 6.3A)

A whole new section, HSDPA Performance Requirements (34.121 Section 9), covers three main test areas:

- Demodulation of HS-DSCH (34.121 9.2)

- Reporting of CQI (34.121 9.3)

- HS-SCCH Detection Performance (34.121 9.4)

The following table lists the most general downlink signal configuration for single-link (non-diversity) scenarios. For simplicity these parameters reflect the minimum requirements from 3GPP TS 25.101 in the specifications, not the relaxed test requirements from 3GPP TS 34.121 that take into account test system uncertainty. Refer to 3GPP TS 34.121 annex E.5.1 and E.6.2 for more information on the general test configuration of the downlink physical channels.

Channel	Level vs. Ior	Notes
P-CPICH	–10 dB	S-CPICH is off (DTX)
P-CCPCH & SCH	–12 dB	Time multiplexed
PICH	–15 dB	
DPCH	Test specific	12.2 k RMC
HS-SCCH-1	Test specific	HS-SCCH-2, 3, 4 are off (DTX)
HS-DSCH (HS-PDSCHs)	Test specific	
OCNS	Remainder	6 channels: 34.121 table E.5.5

Note: The HS-SCCH and the HS-DSCH shall be transmitted continuously (in every TTI) with constant power, but only be allocated to the UE under test during the appropriate TTIs.

Fixed reference channels

Fixed reference channel H-Sets (FRC H-Sets) are the HSDPA equivalent of the reference measurement channels (RMC) used for W-CDMA. The FRC H-Sets define the HS-DSCH configurations most often used for HSDPA conformance testing.

The term "fixed" refers to the static nature of the modulation and coding of these channels. As indicated earlier, AMC is not used because of the difficulty in isolating the performance of the SS from that of the UE.

There are five FRC H-Sets (FRC H-Set 1 to 5) defined in Release 5. Another FRC H-Set (FRC H-Set 6) has been added in Release 6. For some of the tests, such as Demodulation

of HS-DSCH, the UE category determines which FRC H-Set to use:

- FRC H-Set 1 for UE of HS-DSCH category 1 and 2

- FRC H-Set 2 for UE of HS-DSCH category 3 and 4

- FRC H-Set 3 for UE of HS-DSCH category 5 and 6

- FRC H-Set 4 for UE of HS-DSCH category 11

- FRC H-Set 5 for UE of HS-DSCH category 12

- RC H-Set 6 (added in Release 6) and FRC H-Set 3 for UE of HS-DSCH category 7 and 8

HSDPA Transmitter Conformance Tests

Several tests of the transmitter characteristics have been added in the specifications to account for the addition of the HS-DPCCH in the uplink:

- Maximum Output Power with HS-DPCCH (34.121 5.2A)

- Transmit On/Off Power – HS-DPCCH (34.121 5.7A)

- SEM with HS-DPCCH (34.121 5.9A)

- ACLR with HS-DPCCH (34.121 5.10A)

- EVM with HS-DPCCH (34.121 5.13.1A)

The new HSDPA transmitter tests are mainly variations of R99 W-CDMA tests and are used to verify whether the transmitter can handle the addition of the uplink HS-DPCCH. Recall that the HS-DPCCH increases the PAR of the uplink signal, is not transmitted continuously in most cases, and can be offset in time from the DPCCH. These aspects of the HS-DPCCH pose some challenges for the transmitter.

The following HSDPA transmitter conformance tests must therefore be performed with the HS-DPCCH:

- Maximum Output Power test, similar to the standard R99 W-CDMA Maximum Output Power test, but with relaxed output power requirements to enable continued use of R99 power amplifiers with the higher PAR signal

- New power-versus-time mask to verify the accuracy of the uplink power steps when the bursted HS-DPCCH is transmitted (note that the actual test is called "Transmit On/Off Power – HS-DPCCH" in the specifications)

- SEM test and an ACLR test, similar to the standard R99 W-CDMA SEM and ACLR tests, to verify that the transmitter is operating correctly at the reduced maximum output power with the higher PAR signal

- EVM test to verify that the transmitter is operating correctly at the reduced maximum output power with the higher PAR signal. This test should also verify the impact of large HS-DPCCH power steps in the middle of DPCCH/DPDCH slots on the DPCCH/DPDCH signal quality

Test-specific downlink parameters

The following table complements the general downlink test configuration table (Table 1) presented earlier. Here, only the downlink channel configuration test parameters that are specific to the HSDPA
transmitter tests are show

Downlink channels	Level vs. Ior	Notes
DPCH	–9 dB	12.2 k RMC
HS-SCCH-1	–8 dB	HS-SCCH-2, 3, 4 are off (DTX)
HS-DSCH (HS-PDSCHs)	–3 dB	FRC H-Set 1

For these tests, the downlink HS-DSCH is configured as FRC H-Set 1 regardless of the UE category, since FRC H-Set 1 uses an inter-TTI of 3, which all the UE support

The power levels selected for the DPCH, HS-SCCH-1, and HS-DSCH must be high enough to keep the UE's DTX reporting ratio very small and to ensure that the radio link is maintained during the test.

Note that this downlink signal is needed to establish and maintain an HSDPA connection at an inter-TTI interval of 3, but the specific details of the downlink signal configuration are not important for the purpose of transmitter testing and should not affect the results.

Uplink test configuration
All five HSDPA transmitter tests use a similar uplink configuration, which is defined in 3GPP TS 34.121 appendix C.10. One of the objectives of the tests is to verify that HSDPA operation does not interfere with standard operation. For this reason, all the HSDPA tests use a DPCCH and a DPDCH, configured as a standard uplink 12.2 kb/s RMC, in addition to the HS-DPCCH.

In general, a single HS-DPCCH configuration is chosen for all UE categories to limit the number of variables without affecting the results. For example, an inter-TTI interval of 3 is selected because it is supported by all UE categories, even though many are capable of receiving blocks more frequently. A 50% (0.5 slot) time offset between the DPCCH and the HS-DPCCH is used for all tests because this time offset is required for some tests, even though it is unimportant to others.

The code power ratios between the channels in the uplink test configuration depend on which of the six sets of beta factors defined in 3GPP TS 34.121 table C.10.1.4 are used.

In order to simplify the Maximum Output Power, ACLR, and SEM tests, the HS-DPCCH is configured to have continuous power for these tests, as illustrated in Figure 9. Note that these tests are all performed at maximum power.

Figure 15-16   **Generic Uplink Test Signal that is Used for Maximum output power, SEM, and ACLR Tests**
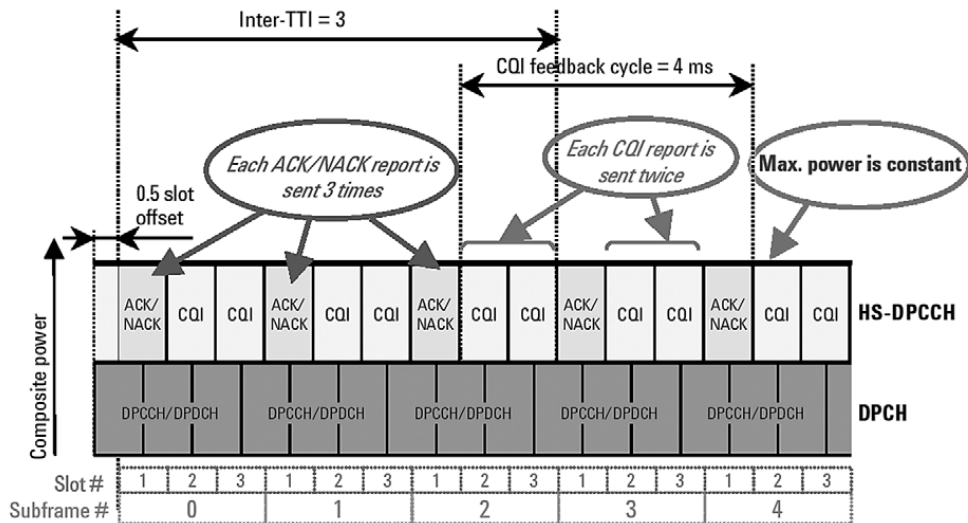
The inter-TTI is 3, so the ACK/NACK repetition factor (N_acknack_transmit) is set to 3 to avoid DTX ACK/NACK fields. The CQI feedback cycle (k) is arbitrarily set to 4 ms and the CQI repetition factor (N_cqi_transmit) is set to 2, which avoids DTX CQI fields.

The power-versus-time (HSDPA Transmit On/Off Power) test uses a more complex uplink signal with discontinuous HS-DPCCH power. As of September 2005, the uplink signal for the EVM test remains undefined but will probably use an HS-DPCCH with a power step.

Transmit On/Off Power – HS-DPCCH (34.121 5.7A)

Power-versus-time (officially called Transmit On/Off Power – HS-DPCCH in the specifications) is an important transmitter test that verifies the accuracy of the power steps caused by the addition of the HS-DPCCH. The transmit power template for this test is given in the following figure. The test is based on a 50% overlap between the DPCCH and the HS-DPCCH timeslots.

Figure 15-17   **Transmit Power Template During Transmit On/Off Power – HS-DPCCH Measurements (ref: 3GPP TS 34.121 figure 5.7A.2).**
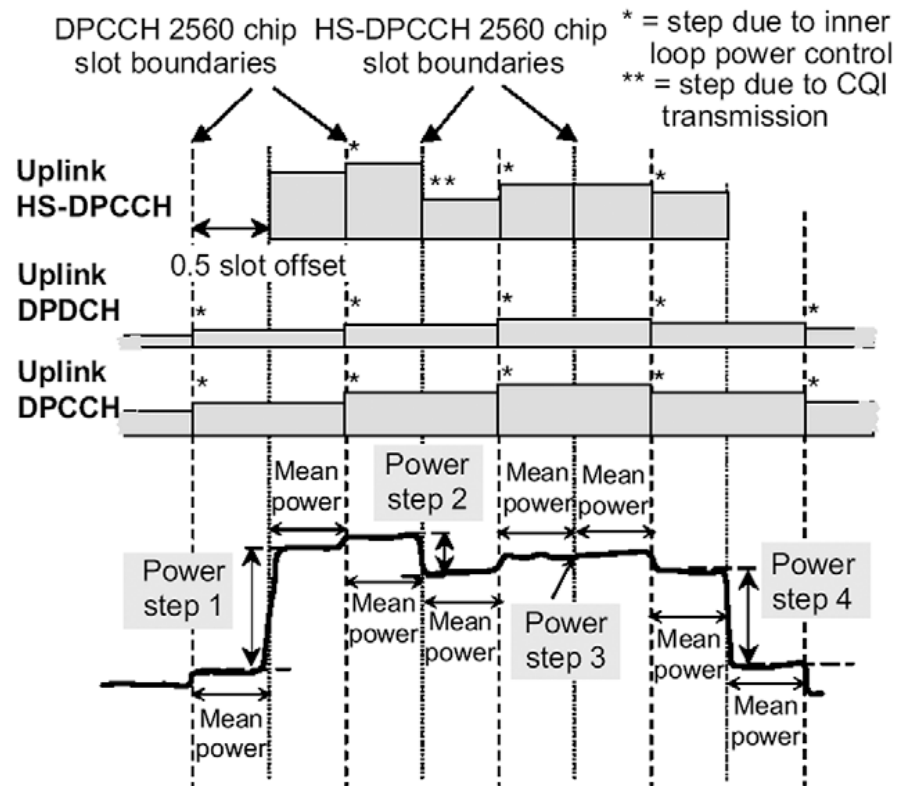
The test considers both the changes in power due to inner loop power control—indicated by an asterisk (*) in Figure 11—and the changes in power due to differences between the relative ACK/NACK and CQI power levels—indicated by two asterisks (**). However, only the accuracy of the latter are measured. The power steps in the ACK/NACK and the CQI boundaries are defined in 3GPP TS 34.121 table 5.7A.2.

The nominal power step due to transmission of ACK/NACK or CQI is defined as the difference between the nominal mean power of any two adjacent power evaluation periods. The HS-DPCCH timeslots are not aligned with the DPCCH timeslots, hence the power evaluation periods are shorter than one timeslot and can be defined in two ways.

- a period that starts with a DPCCH slot boundary and ends with the next HS-DPCCH slot boundary

- a period that starts with an HS-DPCCH slot boundary and ends with the next DPCCH slot boundary

The length of any two adjacent power evaluation periods equals 2560 chips. In all cases the evaluation of mean power must exclude a 25 ms period before and after any DPCCH or HS-DPCCH slot boundary.

According to 3GPP TS 34.121 table 5.7A.2 of the specifications, this test is repeated using the beta factors defined in 3GPP TS 34.121 table C.10.1.4 for sub-tests 5 and 6, which are the most challenging sets in the table.

ACLR and SEM with HS-DPCCH (34.121 5.9A and 5.10A)

ACLR is the power from the carrier that shows up in adjacent and alternate 5 MHz channels. SEM is similar to ACLR but the measurement bandwidth is 30 kHz close in and 1 MHz further out.

The test procedures for ACLR and SEM differ from those of R99 in only one significant way: the HSDPA uplink test signal configuration based on the DPCCH + DPDCH + HS-DPCCH.

EVM with HS-DPCCH (34.121 5.13.1A) and Phase Discontinuity One of the biggest challenges for HSDPA transmitters is to ensure that the UE is transmitting the DPCCH + DPDCH correctly when the HS-DPCCH turns on or off during the DPCCH slot. A possible source of error is the AM to PM distortion caused by having a 7 dB step change in power during a DPCCH slot. If this power step occurs near the UE maximum power level, distortion of the output phase may result, making demodulation by the BTS very difficult.

You can use the existing W-CDMA phase discontinuity measurement to give an indication of whether the performance of a particular UE design is likely to be susceptible to HS-DPCCH power steps.

Under the current W-CDMA requirements, non-HSDPA phase discontinuity is determined by measuring the change in phase between any two adjacent timeslots. Phase transients of up to 30 degrees are allowed only at DPCCH/DPDCH slot boundaries. EVM is measured for each timeslot, excluding the transient periods of 25 µs on either side of the nominal timeslot boundaries. The frequency, absolute phase, absolute amplitude, and chip clock timing used to minimize the error vector are chosen independently for each timeslot. The phase discontinuity result is defined as the difference between the absolute phase used to calculate EVM for the preceding timeslot and the absolute phase used to calculate EVM for the succeeding timeslot.

Downlink configuration of HARQ transmissions

The following table shows the expected behavior of the SS in response to an ACK/NACK, as described in the Demodulation of HS-DSCH conformance test specifications. Here the objective is to simulate the behavior of the Node B. Upon receiving an ACK, the SS must send a new block of data. Upon receiving a NACK, however, it must send a retransmission using the next redundancy version (RV), up to the maximum number of HARQ transmissions allowed. Upon receiving a DTX, the SS must retransmit the same block of data using the same RV previously transmitted for that HARQ process. The RV defines the exact set of bits that are selected during rate-matching (puncturing) to be sent over the air at the time of any one transmission. Thus different RVs represent different puncturing schemes.

HS-DPCCH ACK/NACK field state	Node B emulator behavior
ACK	ACK: new transmission using first redundancy version (RV)
NACK	NACK: retransmission using the next RV (up to the maximum permitted number or RVs)
DTX	DTX: retransmission using the RV previously transmitted to the same HARQ process

The following table shows additional HS-DSCH configuration parameters for the Demodulation of HS-DSCH test. At the most, four HARQ transmissions are allowed, so three retransmissions are allowed. The RV sequence to follow is also specified and depends on the FRC modulation format. For QPSK configurations, RV = 0 is always sent in the first transmission of a block. The RVs 2, 5, and 6 are sent in subsequent retransmissions. For 16QAM configurations, RV = 6 is used for the first transmission and RVs 2, 1, and 5 in subsequent retransmissions. In an FRC all the coding and modulation parameters (except for the RV parameter) are fixed, so the number of bits that are sent over the air is always the same. The only difference between transmissions of the same block using different RVs is which set of bits is sent.

Other HS-DSCH configuration parameters	Value	Notes
Maximum # of HARQ transmissions	4	3 retransmissions allowed
Redundancy/constellation version (RV)	{0, 2, 5, 6}	QPSK configurations
sequence	{6, 2, 1, 5}	16QAM configurations

The following simplified graphic shows the interaction between the SS and the UE during the Demodulation of HS-DSCH test. This example uses FRC H-Set 1 (QPSK), which has two processes and an inter-TTI interval of three.
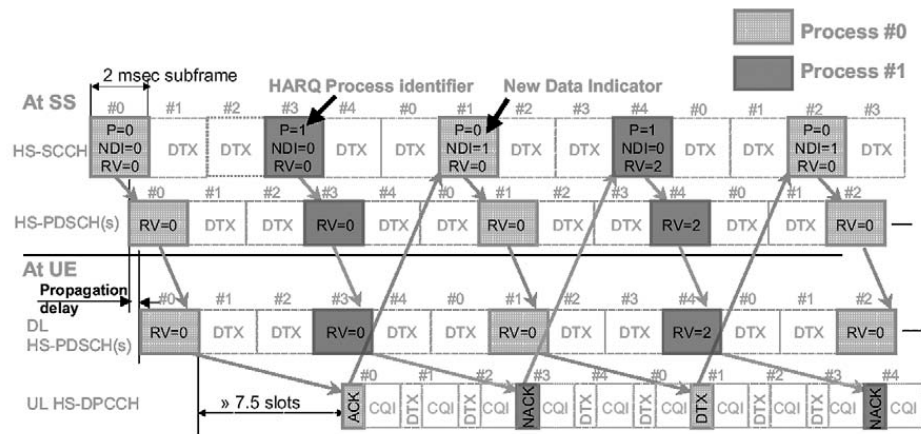
The downlink HS-SCCH indicates that new data is being transmitted from the SS by toggling the new data indicator (NDI) value between 0 and 1 within the same HARQ process (see 3GPP TS 25.321 clause 11.6.1.3). Thus, for a retransmission,

the NDI value stays the same while the RV changes to the next in the sequence. To keep this example simple, we allow a maximum of two HARQ transmissions per block, rather than the four transmissions that are allowed for the actual Demodulation of HS-DSCH test. The RV sequence is {0, 2}.

Note that if a NACK is received for the first block sent for process #1, the SS answers by maintaining the NDI as 0 and changing the RV from 0 to 2. This response indicates that the original data block is being retransmitted using a different RV.

Discontinuous transmission

Code channel amplitude can fluctuate during transmission. This is called DTX or discontinuous transmission. As a result, some bits are lost or not easily demodulate. W-CDMA combats this by replacing the lost bits with Xs so the operator can see which bits are lost.

Select Tri under the Bit Format key to represent the lost bits by an X. Choose the percent of the signal. For example, if 50 percent is chosen and a bit drops off to half of the signal, an X will replace the demodulated bit. The figure below is an example of how Xs are added in place of demodulated bits.

Figure 15-18   X's Used to Replace Demodulated Bits
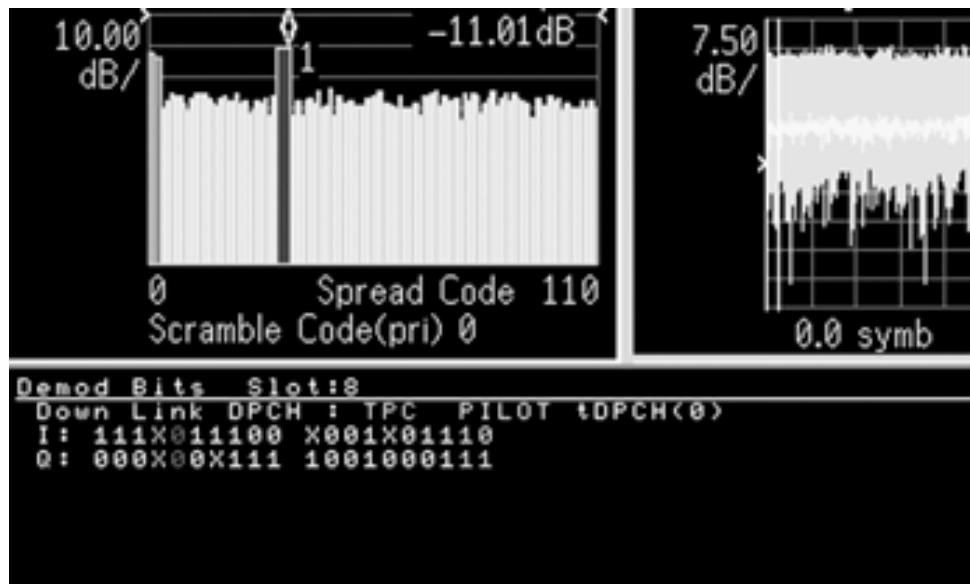
In the 3GPP standard, compressed mode signals have several power-off slots during the transmission. This power-off period prevents active channel identification in code domain. Without identification as active channels, tDPCH (timing offset of DPCH from CPICH) cannot be detected. This means that the slot boundary for a code channel is not correctly identified, which in turn means the demodulation bits and code channel power are affected. Setting tDPCH manually helps to examine the signal in compressed mode correctly because of adjusted slot boundary.

HSUPA Concepts

What is HSUPA?

High Speed Uplink Packet Access (HSUPA) is a digital packet communications format that employs 3GPP-defined Enhanced Data Channels (E-DCH) that support high speed data transmission within the existing W-CDMA communications system. Appropriate uses for HSUPA are UL data bit streams like those employed for digital photography, video, music, games or other high-speed MS applications.

HSUPA is a packet-based data service that supports data transmission rates up to 5.7 Mbps within a 3.84 MHz bandwidth W-CDMA uplink. HSUPA implementations as defined by 3GPP include Soft Handover, Hybrid Automatic Rate reQuest (HARQ), as low as 2ms TTI, and Fast Node B scheduling.

Protocol Structure

The protocol structure of the HSUPA system is the same as the W-CDMA protocol structure. HSUPA employs existing W-CDMA logical channels, but uses different transport and physical layer channels.

Figure 15-19 **W-CDMA Protocol Structure w/ HSUPA Channel Overlay**
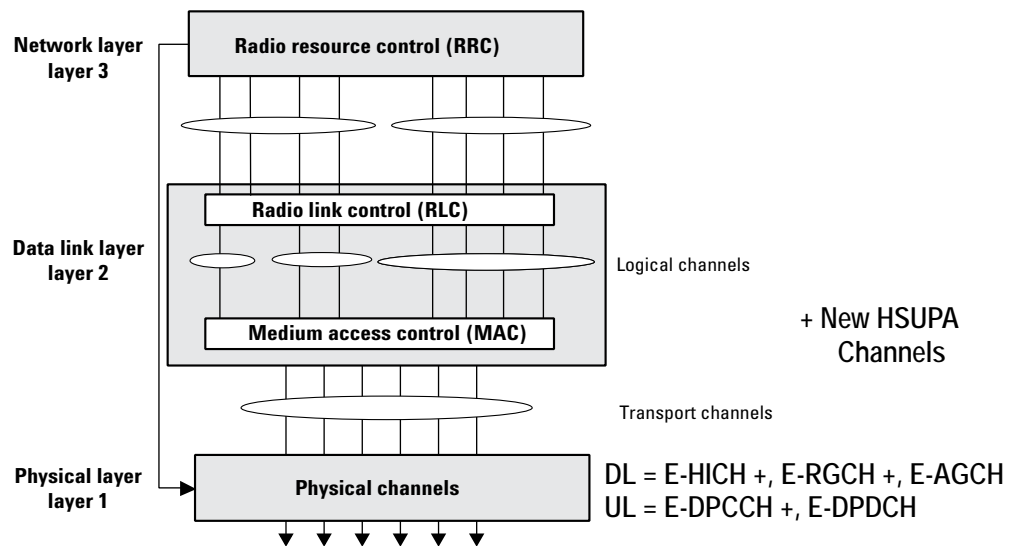
HSUPA Logical, Transport, and Physical Channels

HSUPA cooperates with existing W-CDMA transport channels to support sharing physical resources between multiple services. Each service, such as data, fax, voice, or signaling, is routed into different transport channels by the upper signaling layers. These services may have different data rates and error control schemes. The transport channels are then multiplexed as required prior to transmission via one or more physical channels. High data rate services or a combination of lower rate transport channels are then multiplexed into several physical channels.

HSUPA also cooperates with the W-CDMA UL and DL physical channels. The most important UL physical channel used by HSUPA is the Dedicated Physical Control Channel (DPCCH). .

HSUPA Downlink E-CDH Physical Channels

E-CDH Absolute Grant Channel (E-AGCH)

The E-CDH Absolute Grant Channel (E-AGCH) is a shared channel created for HSUPA to control E-DPDCH absolute transmissions. The E-AGCH is for downlink signaling and associated scheduling from the serving cell only. The serving E-DCH cell is the one from which the UE receives Absolute Grants from the Node-B scheduler. A UE has only one serving E-DCH cell. For more information see "HSUPA Cell Connection Overview" on page 137.

The E-AGCH is a fixed rate (30kbps, SF=256) downlink physical channel carrying the uplink E-DCH absolute grant. Figure 15-20 illustrates the frame and subframe structure of the E-AGCH.

Figure 15-20   Sub-structure for E-AGCH
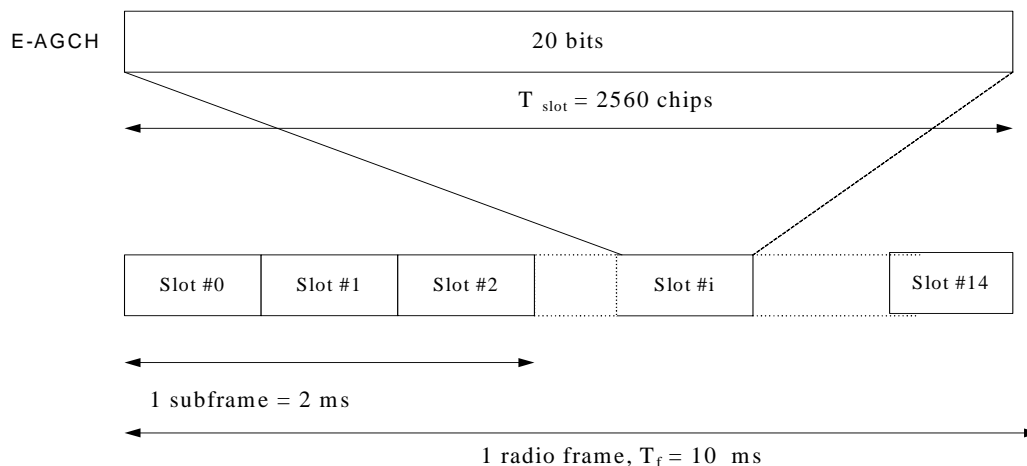
An E-DCH absolute grant is transmitted over one E-AGCH sub-frame or one E-AGCH frame. The transmission over one E-AGCH sub-frame and over one E-AGCH frame is used for UEs for which E-DCH TTI is set to 2 ms and 10 ms respectively. See Figure 15-21.

Figure 15-21   Channel Coding for E-AGCH

$X_{ag,1}$, X_{ag2},…, $X_{ag,6}$

ID specific
CRC attachment

Y_1, Y_2,…, Y_{22}

Channel coding

Z_1, Z_2,…, Z_{90}

Rate Matching

F_1, F_2,…, F_{60}

Physical Channel
mapping

E-AGCH
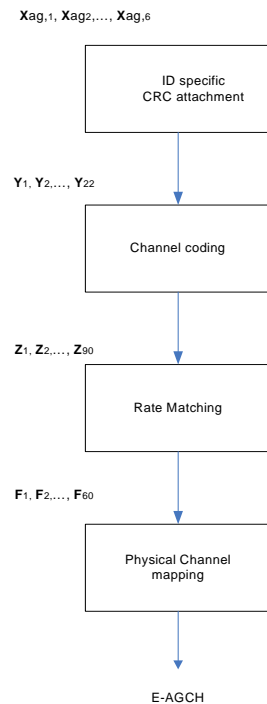
E-CDH HARQ Indicator Channel (E-HICH)

The E-CDH HARQ Indicator Channel (E-HICH) is a dedicated channel created for HSUPA to carry HARQ Feedback to the UE. The E-HICH is for associated ACK/NACK signaling from the Node B.

The E-DCH Hybrid ARQ Indicator Channel (E-HICH) is a fixed rate (SF=128) dedicated downlink physical channel carrying the uplink E-DCH hybrid ARQ acknowledgement indicator.

A hybrid ARQ acknowledgement indicator is transmitted using 3 or 12 consecutive slots. In each slot a sequence of 40 binary values is transmitted. The 3 and 12 slot duration periods are used for UEs, for which the E-DCH TTI is set, respectively, to 2 ms and 10 ms.

In a radio link set (RLS) containing the serving E-DCH radio link set, the hybrid ARQ acknowledgement indicator a is set to +1 or –1 (ACK or NACK), and in a radio link set not containing the serving E-DCH radio link set the hybrid ARQ indicator is set to +1 or 0 (ACK or NACK).

Table 15-2 **Mapping of HARQ Acknowledgement**

Command	HARQ acknowledgement indicator
ACK	+1
NACK (RLSs not containing the serving E-CDH cell)	0
NACK (RLSs containing the serving E-CDH cell)	−1

For more information see "HSUPA Cell Connection Overview" on page 137.

E-CDH Relative Grant Channel (E-RGCH)

The E-CDH Relative Grant Channel (E-RGCH) is a dedicated channel created for HSUPA to control E-DPDCH relative transmissions. The E-RGCH is used for downlink signaling and associated scheduling from the E-DCH active set. The E-DCH active set is the set of cells which carry the E-DCH for one UE. The E-DCH Relative Grant Channel (E-RGCH) is a fixed rate (SF=128) dedicated downlink physical channel carrying the uplink E-DCH relative grants. Figure 15-22 on page 128 illustrates the structure of the E-RGCH.

Figure 15-22 **E-RGCH and E-HICH structure**
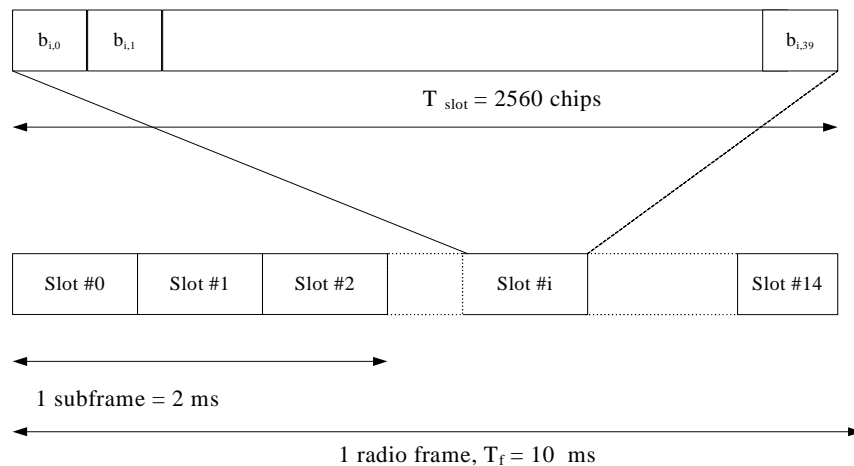
A relative grant is transmitted using 3, 12, or 15 consecutive slots. In each slot a sequence of 40 ternary values is transmitted. The 3 or 12 slot duration is used on an

E-RGCH transmitted to UEs when the cell transmitting the E-RGCH is in the E-DCH serving radio link set (RLS), and when the E-DCH TTI is respectively 2 and 10 ms. The 15 slot duration is used on an E-RGCH transmitted to UEs when the cell transmitting the E-RGCH is not in the E-DCH serving radio link set. In a serving E-DCH radio link set, the relative grant value is set to +1, 0, or -1 (Up, Hold, or Down). In a radio link not belonging to the serving E-DCH radio link set, the relative grant value is set to 0 or -1 (Hold or Down).

Table 15-3   Mapping of Relative Grant (RG) Values

Command	RG Value (serving E-DCH RLS)	RG Value (other radio links)
UP	+1	Not Allowed
HOLD	0	0
DOWN	−1	−1

For more information see "HSUPA Cell Connection Overview" on page 137.

HSUPA Uplink Physical Channels

The Dedicated Physical Channel (DPCH) is used for HSDPA in the same manner as for other W-CDMA traffic. It carries all the user data and user signaling, as well as physical channel control bits for the slot format and the UE inner loop power control. The DPCH consists of the DPDCH and the DPCCH. The user's digitized voice and/or digital data, along with layer 3 signaling data, are carried on the DPDCH. The user data and signaling data are individually treated with error protection coding and interleaving, then multiplexed together to form the DPDCH. The DPDCH is then multiplexed with the DPCCH, which contains the Transmit Power Control (TPC) bits (to control the UE transmit power), Transport Format Combination Indicator (TFCI) bits (indicates the slot format and data rate), and embedded Pilot bits (short synchronization patterns embedded within each slot).

A maximum of 6 DPDCH and 1 HS-DPCCH channels may be used in an uplink transmission in what is known as HSUPA Configuration 1. See "Allowable HSUPA Uplink Physical Channel Configurations" on page 135.

E-CDH Dedicated Physical Control Channel (E-DPCCH)

The E-CDH Dedicated Physical Control Channel (E-DPCCH) is a dedicated channel created for HSUPA that carries control information associated with the E-CDH. There is, at most, one E-DPCCH on each radio uplink. See "Allowable HSUPA Uplink Physical Channel Configurations" on page 135.

Figure 15-23   E-DPDCH Frame Structure

The frame and sub-frame structure of E-DPCCH is shown in Figure 15-23. Each E-DPCCH radio frame is divided into 5 subframes, where each subframe is 2 ms in

E-DPDCH frame structure
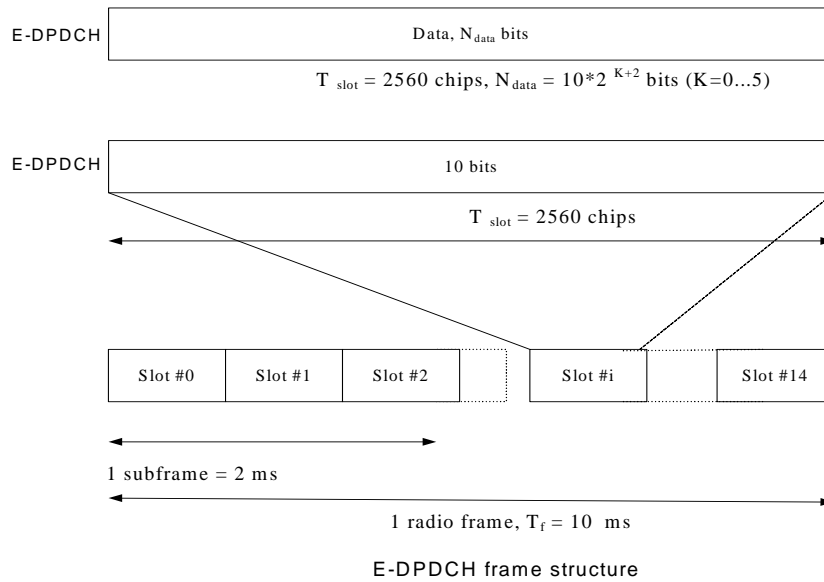
length; the first subframe starts at the start of each radio frame and the 5th subframe ends at the end of each radio frame. The E-DPCCH is not transmitted in a slot unless the DPCCH is also transmitted in the same slot. The E-DPCCH slot format (only 0 is available) is shown in Table 15-4.

Table 15-4   E-DPCCH Slot Format

Slot Format #i	Channel Bit Rate (kbps)	SF	Bits/ Frame	Bits/ Subframe	Bits/Slot N_{data}
0	15	256	150	30	10

The following information is transmitted by means of the E-DPCCH physical channel:

- Retransmission Sequence Number (RSN) (2bits) - To indicate the redundancy version (RV) of each HARQ transmission and to assist the Node B soft buffer management, a two bit RSN is signaled from the UE to the Node B. The Node B can avoid soft buffer corruption by flushing the soft buffer associated to one HARQ process, in case more than 3 consecutive E DPCCH transmissions in that HARQ process can not be decoded, or the last received RSN is incompatible with the current one.

- E-TFCI information (7bits)

- "Happy" bit (1bit) - This is a single bit field that is passed from MAC to the physical layer for inclusion on the E-DPCCH. This field takes two values, "Not Happy" and "Happy", indicating respectively whether the UE could use more resources or not: whether or not the UE is satisfied ('happy') or not ('not happy') with the current Serving Grant.

Figure 15-24 shows the coding chain for the E-DPCCH channel.

Figure 15-24 **Coding Chain for E-DPCCH**

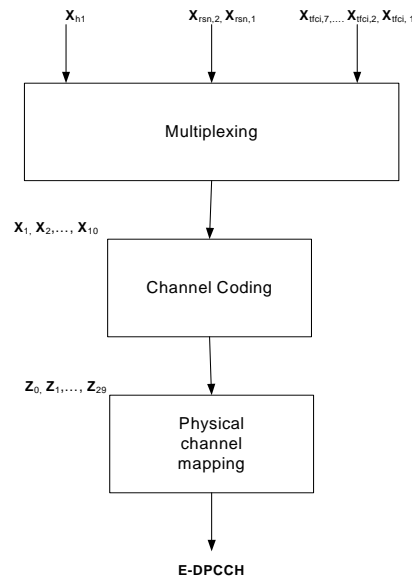**E-DCH Dedicated Physical Data Channel (E-DPDCH)**

The E-CDH Dedicated Physical Data Channel (E-DPDCH) is a dedicated channel created for HSUPA that carries uplink data. There are at most four E-DPDCH channels on each radio uplink. See "Allowable HSUPA Uplink Physical Channel Configurations" on page 135.

The frame and subframe structure of E-DPDCH is shown in Figure 15-23 on page 129. The E-DPDCH and the E-DPCCH are always transmitted simultaneously, except in the case that E-DPDCH is DTXed, but E-DPCCH is not DTXed, due to power scaling. The E-DPDCH slot formats, corresponding rates, and number of bits are shown in Table

Table 15-5 **E-DPDCH Slot Formats**

Slot Format #i	Channel Bit Rate (kbps)	SF	Bits/ Frame	Bits/ Subframe	Bits/Slot N_{data}
0	15	256	150	30	10
1	30	128	300	60	20
2	60	64	600	120	40
3	120	32	1200	240	80
4	240	16	2400	480	160
5	480	8	4800	960	320
6	960	4	9600	1920	640
7	1920	2	19200	3840	1280

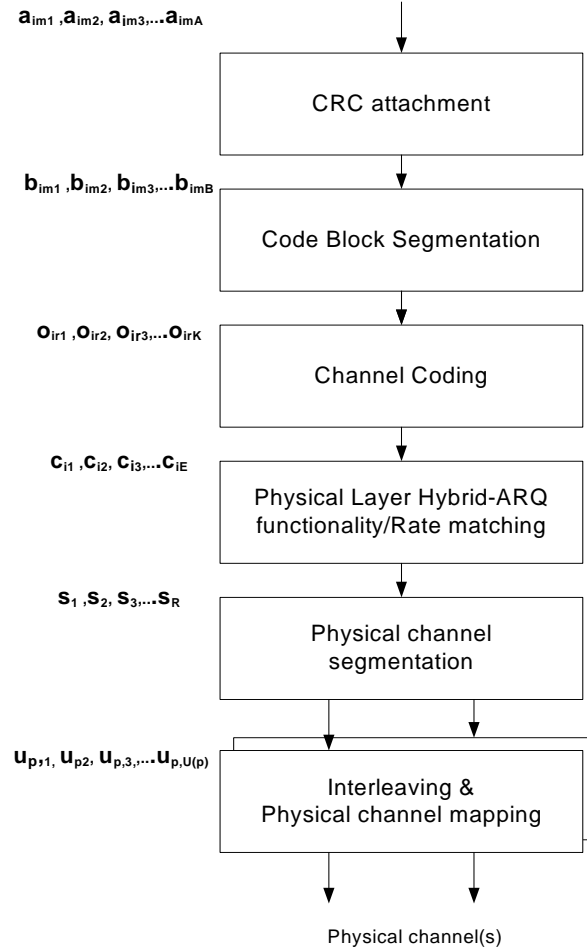The output of "Physical channel segmentation" can be multiple E-DPDCH code

channels. In this way, an E-DCH transport channel can be mapped to two or more physical E-DPDCH channels in each radio uplink in order to support higher packet data rates.

Figure 15-25   **Transport Channel Processing for E-DCH**

$a_{im1}, a_{im2}, a_{im3}, ... a_{imA}$

CRC attachment

$b_{im1}, b_{im2}, b_{im3}, ... b_{imB}$

Code Block Segmentation

$o_{ir1}, o_{ir2}, o_{ir3}, ... o_{irK}$

Channel Coding

$c_{i1}, c_{i2}, c_{i3}, ... c_{iE}$

Physical Layer Hybrid-ARQ
functionality/Rate matching

$s_1, s_2, s_3, ... s_R$

Physical channel
segmentation

$u_{p,1}, u_{p2}, u_{p,3}, ... u_{p,U(p)}$

Interleaving &
Physical channel mapping

Physical channel(s)

In addition to Figure 15-24 on page 131, which shows Uplink DPDCH/DPCCH coding, spreading, and scrambling, and Figure 15-11 on page 107, which shows Uplink DPDCH/HS-DPCCH coding, spreading, and scrambling, the input summation block, as shown in Figure 15-26 on page 134, illustrates spreading, gain factor weighting, and the I/Q branch mapping that is used on the UL E-DCH.

Figure 15-26   **Spreading for E-DPDCH/E-DPCCH**
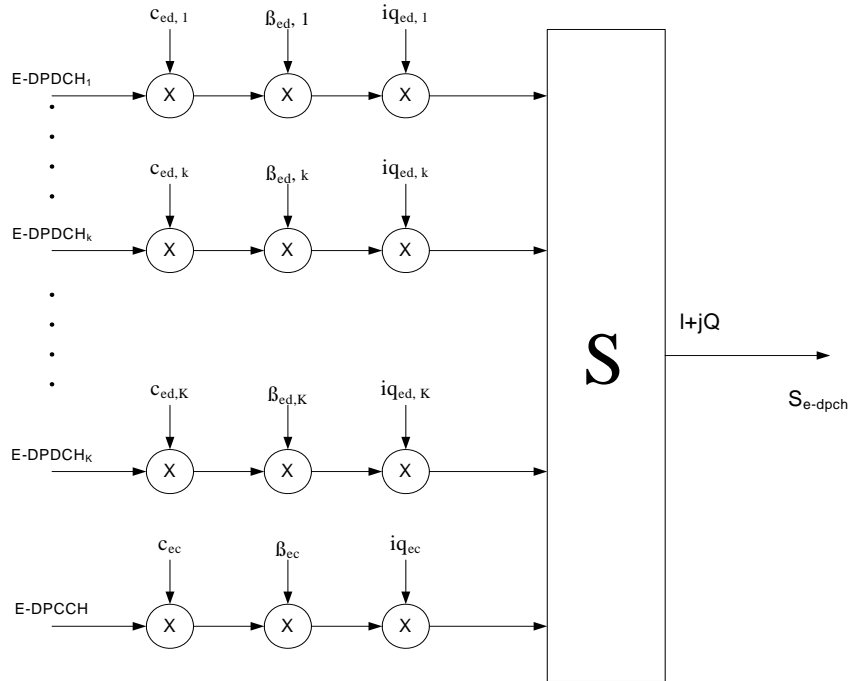
The E-DPCCH is spread to the chip rate by the channelization code c_{ec}. The *k*-th E-DPDCH, denominated "E-DPDCH$_k$", is spread to the chip rate using channelization code $c_{ed.k.}$ After channelization, the real-valued spread E-DPCCH and E-DPDCH$_k$ signals are respectively weighted by gain factors β_{bec} and $\beta_{ed.k}$

After weighting, the real-valued spread signals are mapped to the I or Q branch, according to the iq_{ec} value for the E-DPCCH and the $iq_{ed.k}$ value for the E-DPDCH$_k$, which are then summed together. The E-DPCCH is always mapped to the I branch. The IQ branch mapping for the E-DPDCHs depends on $N_{max-dpdch}$, and on whether an HS-DSCH (HS-DPCCH) is configured for the UE; the possible HSUPA physical channel configurations, including IQ branch mapping, with or without the DPCH (conventional W-CDMA) or HS-DSCH (HSDPA), are shown in "Allowable HSUPA Uplink Physical Channel Configurations" on page 135.

HSUPA Dedicated Physical Channel Uplink Configurations

In addition to the DPCCH/DPDCH and the HS-DPCCH, all allowed HSUPA uplink channel configurations permitted by 3GPP Release 6 are shown in the Table , "HSUPA Cell Connection Overview," on page 137.

The following configurations are also used to set up the DPCH Configuration for the Code Domain Power measurement of an HSUPA signal. The **DPCH/E-DPCH Config** menu is part of the **Meas Setup** menu for the Code Domain Measurement.
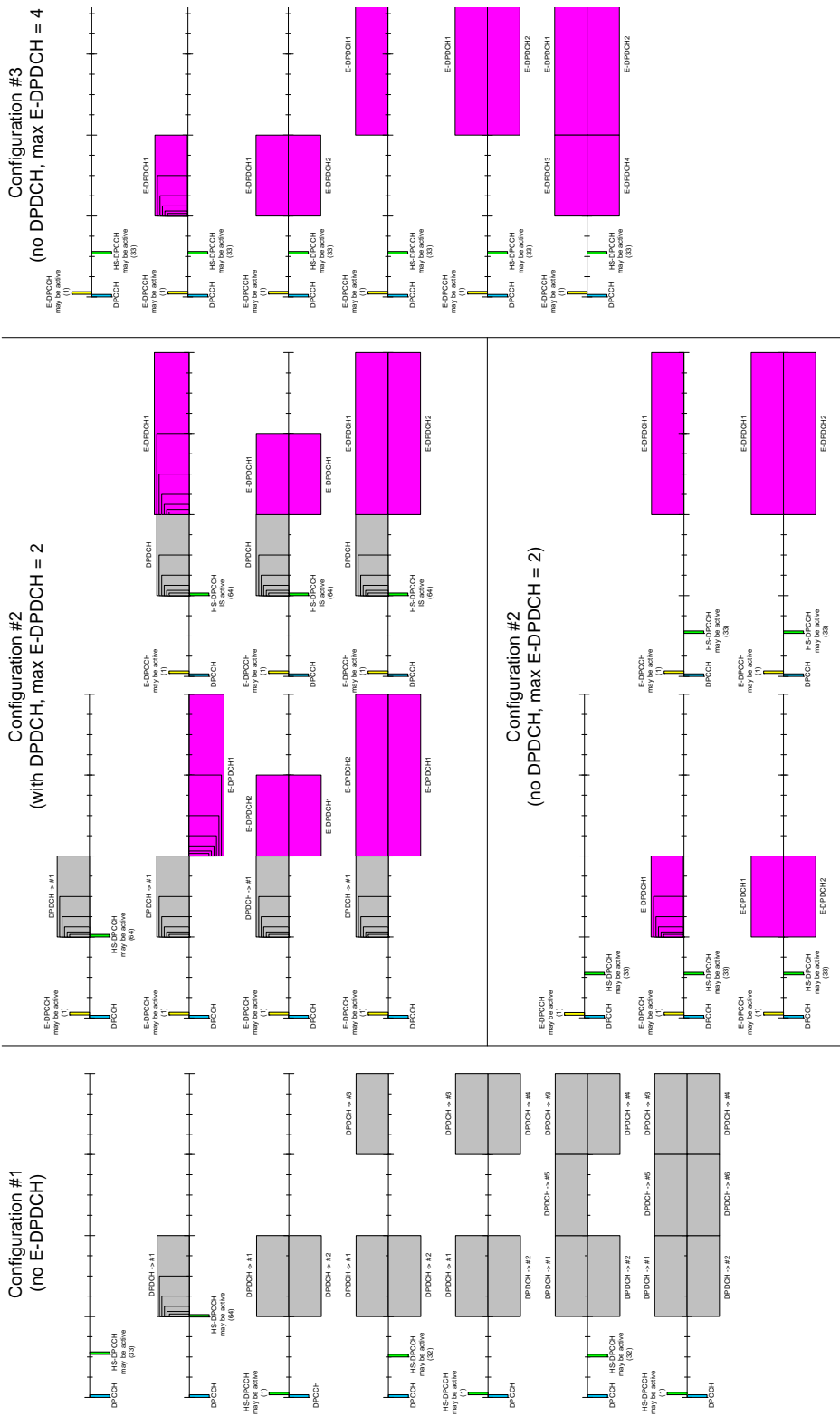
Table 15-6   **Allowable HSUPA Uplink Physical Channel Configurations**

Configuration Number	DPDCH	HS-DPCCH	E-DPDCH	E-DPCCH
1	6	1	0	0
2	1	1	2	1
2 (no DPDCH)	0	1	2	1
3	0	1	4	1

Figure 15-27   HSUPA DPCH/E-DPCH Code Domain Channels by Configuration Number

HSUPA Uplink Data Rates

HSUPA achieves various data rates as required by varying the number of data channels and their respective spreading factors. The maximum theoretical data rate that can be attained with HSUPA is 5.76 Mbps, using the maximum number of data channels and the highest spreading factors, as shown in the table below.

Table 15-7   **HSUPA Effective Data Rates in Mbps by Channels Used and SF**

Effective Coding Rate	Number of Data Channels / Spreading Factor (SF)			
	1 @ SF4	2 @ SF4	2 @ SF2	2 @ SF4 + 2 @ SF2
1/2	480 Mbps	960 Mbps	1920 Mbps	2880 Mbps
3/4	720 Mbps	1440 Mbps	2880 Mbps	4320 Mbps
4/4	950 Mbps	1920 Mbps	3840 Mbps	5760 Mbps

Details of the code domain channel assignments for each of the various data channel configurations are shown in .

HSUPA Cell Connection Overview

In and the following E-DCH conditions apply:

- E-DCH active set: The set of cells which carry the E-DCH for one UE.

- Serving E-DCH Cell: Cell from which the UE receives Absolute Grants from the Node-B scheduler. A UE has one Serving E-DCH Cell.

- Serving E-DCH Radio Link Set (RLS): Set of cells which contain at least a Serving E-DCH cell, from which the UE can receive and combine one Relative Grant. The UE has only one Serving E-DCH RLS. This is also called a "Serving RLS".

- Non-Serving E-DCH Radio Link (RL): Cell which belongs to the E-DCH active set but does not belong to the Serving E-DCH RLS; the UE can receive one Relative Grant from this cell. The UE can have zero, one or several Non-serving E-DCH RL(s). This is also called a "Non-serving RL".

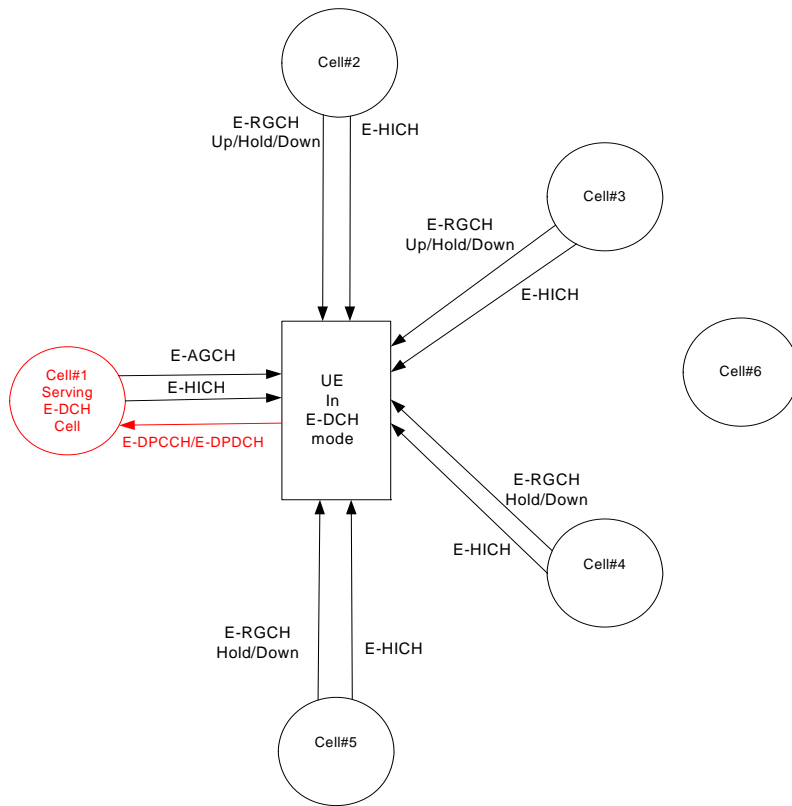**Figure 15-28**   **HSUPA Cell Connection Diagram**

Table 15-8   **HSUPA Cell Connections**

Cell Number	E-DCH Active Set?	Serving E-DCH RLS?	Non-serving E-DCH RL?
1 (Serving E-DCH cell)	X	X	
2	X	X	
3	X	X	
4	X		X
5	X		X
6			

Where:

- **E-DCH active set:** The set of cells that carry the E-DCH for one UE.

- **Serving E-DCH cell:** The cell from which the UE receives Absolute Grants

from the Node-B scheduler. A UE has one Serving E-DCH cell.

- **Serving E-DCH Radio Link Set (RLS)**: The set of cells that contain at least the Serving E-DCH cell and from which the UE can receive and combine one Relative Grant. The UE has only one Serving E-DCH RLS (also called the "Serving RLS).

- **Non-Serving E-DCH Radio Link (RL):** A cell which belongs to the E-DCH active set but does not belong to the Serving E-DCH RLS, and from which the UE can receive one Relative Grant. The UE can have zero, one, or several Non-serving E-DCH RLs (also called the "Non-serving RLS").

Time Gating Concepts

Common file used in SA, WiMAX, & W-CDMA measurement guide.

Introduction: Using Time Gating on a Simplified Digital Radio Signal

This section shows you the concepts of using time gating on a simplified digital radio signal. The section on Making Time-Gated Measurements demonstrates time gating examples.

Figure 2. shows a signal with two radios, radio 1 and radio 2, that are time-sharing a single frequency channel. Radio 1 transmits for 1 ms then radio 2 transmits for 1 ms.

Figure 2.   Simplified Digital Mobile-Radio Signal in Time Domain
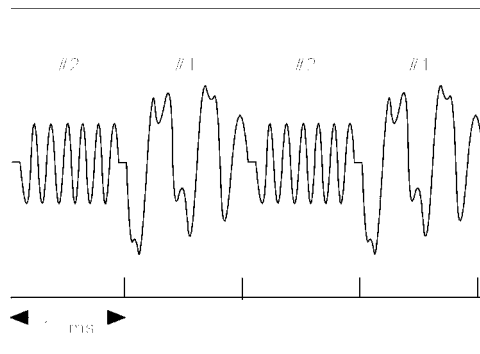
We want to measure the unique frequency spectrum of each transmitter.

A signal analyzer without time gating cannot do this. By the time the signal analyzer has completed its measurement sweep, which lasts about 50 ms, the radio transmissions switch back and forth 25 times. Because the radios are both transmitting at the same frequency, their frequency spectra overlap, as shown in Figure 3. The signal analyzer shows the combined spectrum; you cannot tell which part of the spectrum results from which signal.

Figure 3.   Frequency Spectra of the Combined Radio Signals
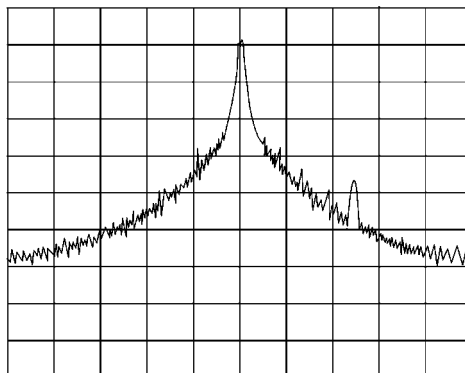
Time gating allows you to see the separate spectrum of radio 1 or radio 2 to determine the source of the

spurious signal, as shown in Figure 4.

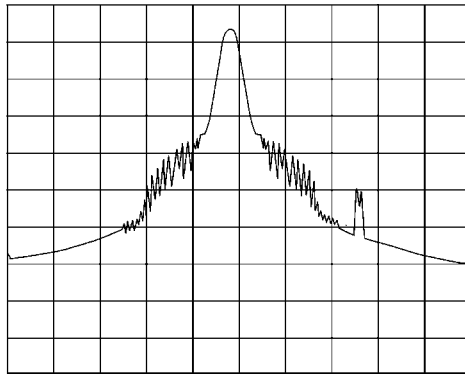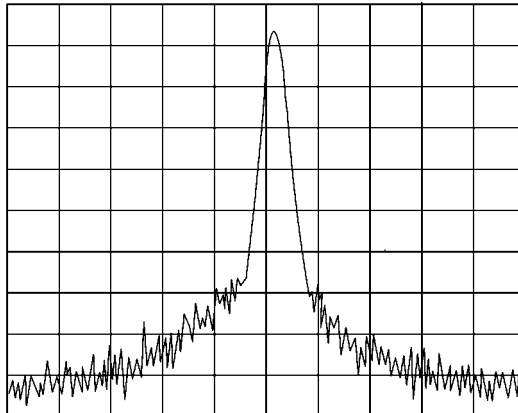**Figure 4.   Time-Gated Spectrum of Radio 1**

Figure 5.   Time-Gated Spectrum of Radio 2

Time gating lets you define a time window (or time gate) of when a measurement is performed. This lets you specify the part of a signal that you want to measure, and exclude or mask other signals that might interfere.

How Time Gating Works

Time gating is achieved by the signal analyzer selectively interrupting the path of the detected signal, with a gate, as shown in Figure 8. and Figure 7. The gate determines the times at which it captures measurement data (when the gate is turned "on," under the Gate menu, the signal is being passed, otherwise when the gate is "off," the signal is being blocked). Under the right conditions, the only signals that the analyzer measures are those present at the input to the analyzer when the gate is on. With the correct signal analyzer settings, all other signals are masked out.

There are typically two main types of gating conditions, *edge* and *level*:

*   With edge gating, the gate timing is controlled by user parameters (gate delay and gate length) following the selected (rising or falling) edge of the trigger signal. The gate passes a signal on the edge of the trigger signal (after the gate delay time has been met) and blocks the signal at the end of the gate length.

    With edge gating, the gate control signal is usually an external periodic TTL signal that rises and falls in synchronization with the rise and fall of the pulsed radio signal. The gate delay is the time the analyzer waits after the trigger event to enable the gate (see Figure 6.).

*   With level gating, the gate will pass a signal when the gate signal meets the specified level (high or low). The gate blocks the signal when the level conditions are no longer satisfied (level gating does not use gate length or gate delay parameters).

Figure 6.   Edge Trigger Timing Relationships
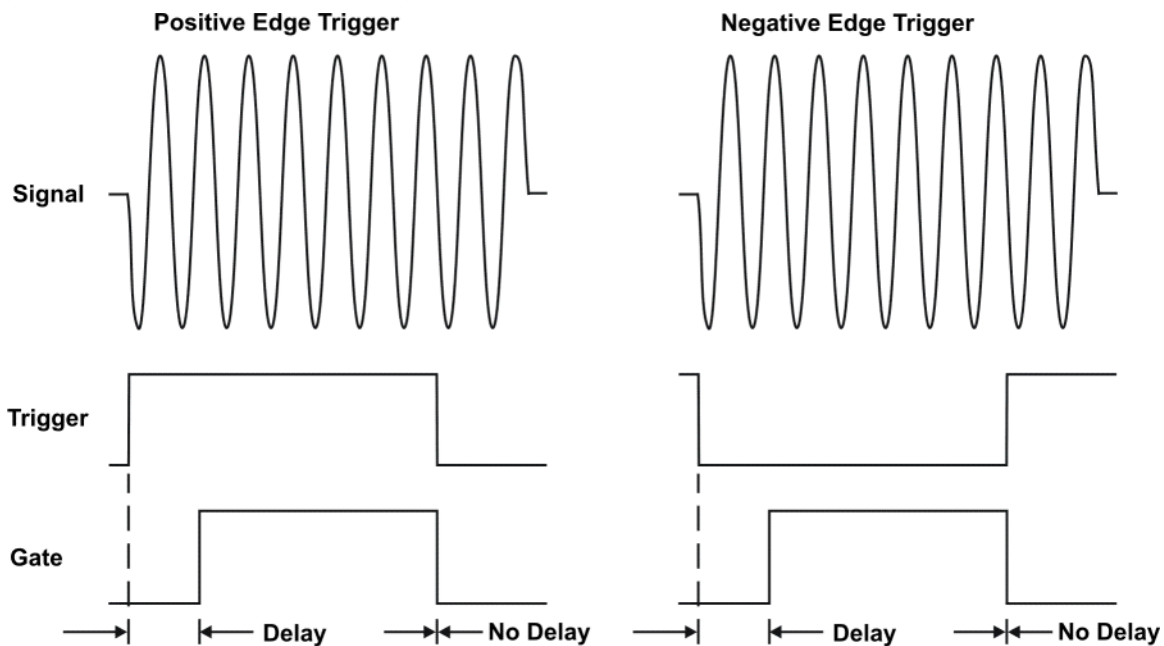
With Agilent signal analyzers, there are three different implementations for time gating: gated LO, gated video and gated FFT.

Gated Video Concepts

Gated video may be thought of as a simple gate switch, which connects the signal to the input of the signal analyzer. When the gate is "on" (under the Gate menu) the gate is passing a signal. When the gate is "off," the gate is blocking the signal. Whenever the gate is passing a signal, the analyzer sees the

signal. In Figure 7. notice that the gate is placed after the envelope detector and before the video bandwidth filter in the IF path (hence "gated video").

The RF section of the signal analyzer responds to the signal. The selective gating occurs before the video processing. This means that there are some limitations on the gate settings because of signal response times in the RF signal path.

With video gating the analyzer is continually sweeping, independent of the position and length of the gate. The analyzer must be swept at a minimum sweep time (see the sweep time calculations later in this chapter) to capture the signal when the gate is passing a signal. Because of this, video gating is typically slower than gated LO and gated FFT.

Figure 7.   Gated Video Signal Analyzer Block Diagram
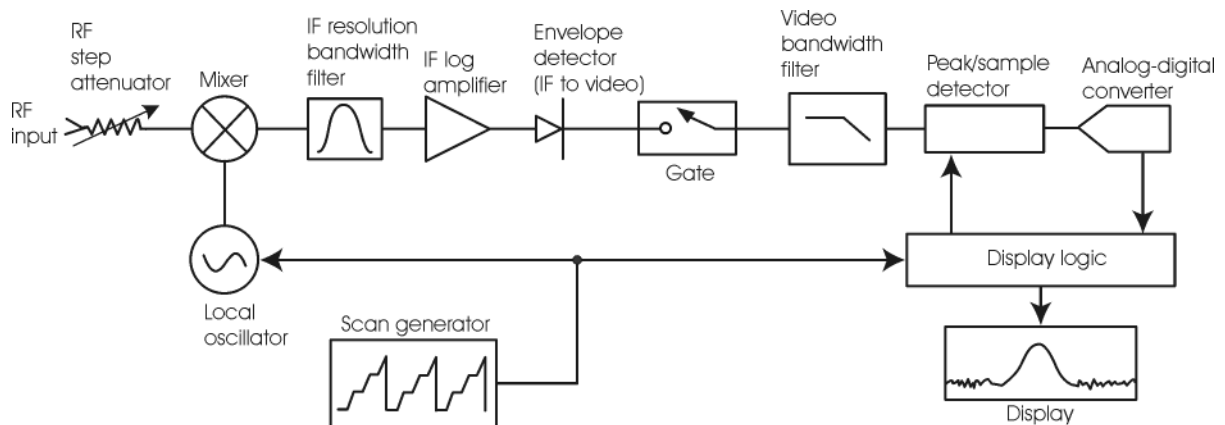
Gated LO Concepts

Gated LO is a very sophisticated type of time gating that sweeps the LO only while the gate is "on" and the gate is passing a signal. See Figure 8. for a simplified block diagram of gated LO operation. Notice that the gate control signal controls when the scan generator is sweeping and when the gate passes or blocks a signal. This allows the analyzer to sweep only during the periods when the gate passes a signal. Gated LO is faster than Gated Video because Gated Video must constrain sweep time so that each point is long enough to include a burst event. On the other hand, when in Gated LO, multiple points may be swept during each gate.

Figure 8.   Gated LO Signal Analyzer Block Diagram
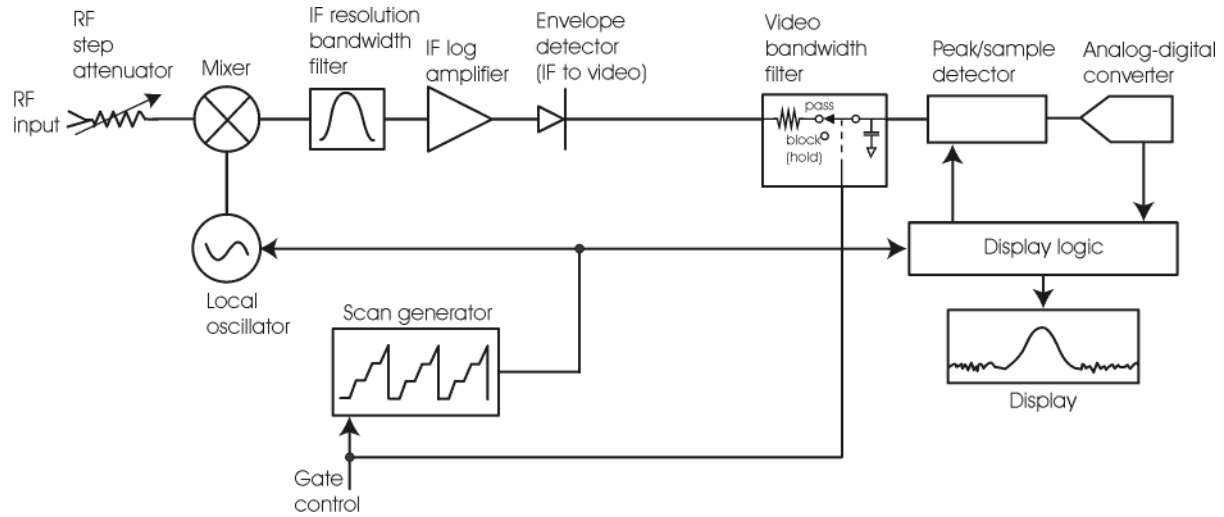
Gated FFT Concepts

Gated FFT (Fast-Fourier Transform) is an FFT measurement which begins when the trigger conditions are satisfied.

The process of making a spectrum measurement with FFTs is inherently a "gated" process, in that the spectrum is computed from a time record of short duration, much like a gate signal in swept-gated analysis.

Using the analyzer in FFT mode, the duration of the time record to be gated is:

$$\text{FFT Time Record (to be gated)} = \frac{1.83}{\text{RBW}}$$

The duration of the time record is within a tolerance of approximately 3% for resolution bandwidths up through 1 MHz. Unlike swept gated analysis, the duration of the analysis in gated FFT is fixed by the RBW, not by the gate signal. Because FFT analysis is faster than swept analysis (up to 7.99 MHz), the gated FFT measurements can have better frequency resolution (a narrower RBW) than swept analysis for a given duration of the signal to be analyzed.

Figure 9. **Gated FFT Timing Diagram**
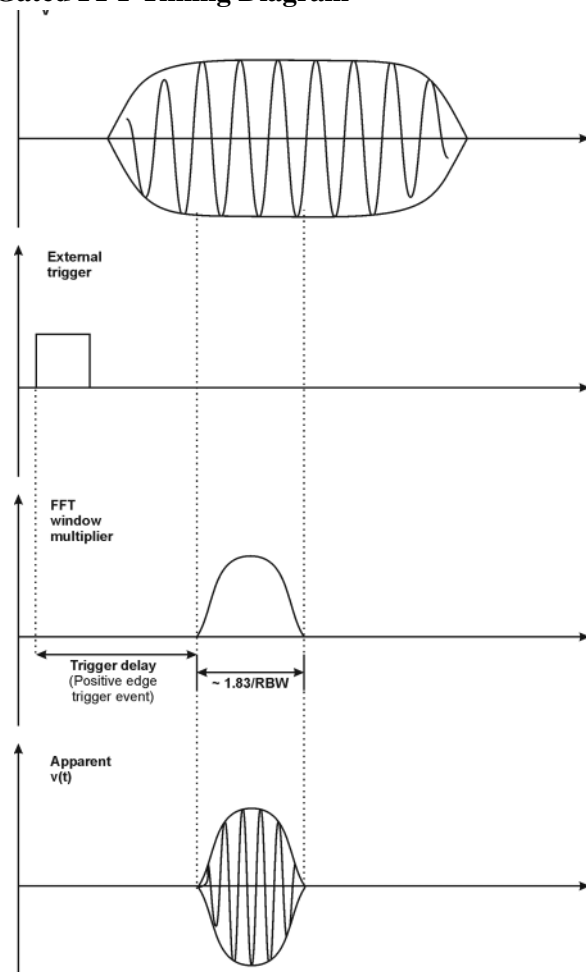
Time Gating Basics (Gated LO and Gated Video)

The gate passes or blocks a signal with the following conditions:

- Trigger condition - Usually an external transistor-transistor logic (TTL) periodic signal for edge triggering and a high/low TTL signal for level triggering.

- Gate delay - The time after the trigger condition is met when the gate begins to pass a signal.

- Gate length - The gate length setting determines the length of time a gate begins to pass a signal.

To understand time gating better, consider a spectrum measurement performed on two pulsed-RF signals sharing the same frequency spectrum. You will need to consider the timing interaction of three signals with this example:

- The composite of the two pulsed-RF signals.

- The gate trigger signal (a periodic TTL level signal).

- The gate signal. This TTL signal is low when the gate is "off" (blocking) and high when the gate is "on" (passing).

The timing interactions between the three signals are best understood if you observe them in the time

domain (see Figure 10.).

The main goal is to measure the spectrum of signal 1 and determine if it has any low-level modulation or spurious signals.

Because the pulse trains of signal 1 and signal 2 have almost the same carrier frequency, their spectra overlap. Signal 2 will dominate in the frequency domain due to its greater amplitude. Without gating, you won't see the spectrum of signal 1; it is masked by signal 2.

To measure signal 1, the gate must be on only during the pulses from signal 1. The gate will be off at all other times, thus excluding all other signals. To position the gate, set the gate delay and gate length, as shown in Figure 10., so that the gate is on only during some central part of the pulse. Carefully avoid positioning the gate over the rising or falling pulse edges. When gating is activated, the gate output signal will indicate actual gate position in time, as shown in the line labeled "Gate."

Figure 10.   Timing Relationship of Signals During Gating
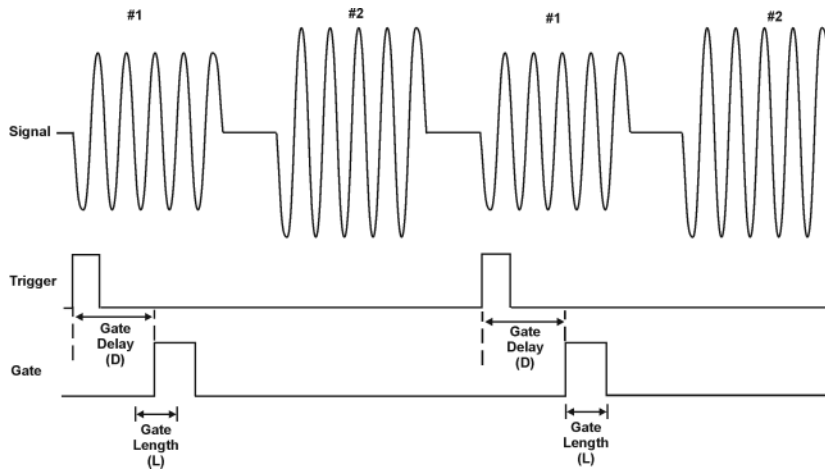
Once the signal analyzer is set up to perform the gate measurement, the spectrum of signal 1 is visible and the spectrum of signal 2 is excluded, as shown if Figure 12. In addition, when viewing signal 1, you also will have eliminated the pulse spectrum generated from the pulse edges. Gating has allowed you to view spectral components that otherwise would be hidden.

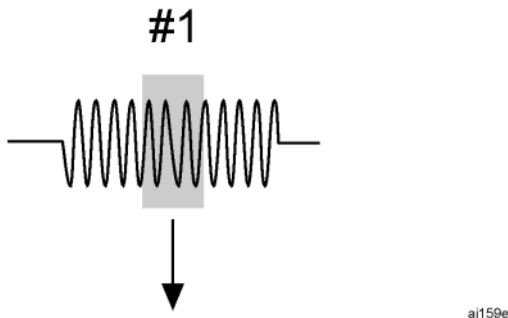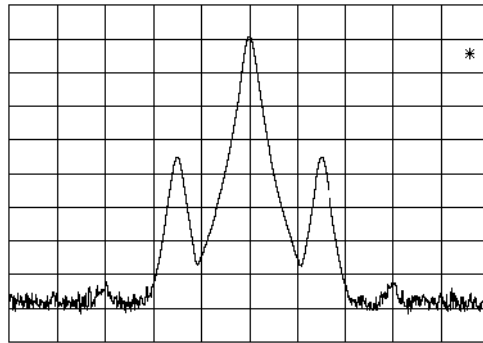**Figure 11.   Signal within pulse #1 (time-domain view)**

Figure 12. **Using Time Gating to View Signal 1 (spectrum view)**

Moving the gate so that it is positioned over the middle of signal 2 produces a result as shown in Figure 14. Here, you see only the spectrum within the pulses of signal 2; signal 1 is excluded.

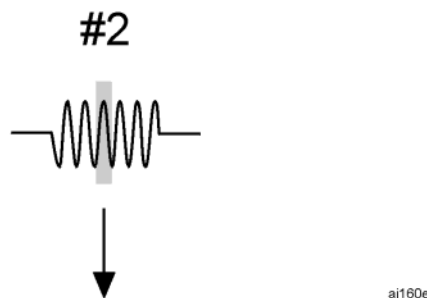**Figure 13.** **Signal within pulse #2 (time-domain view)**

Figure 14. **Using Time Gating to View Signal 2 (spectrum view)**
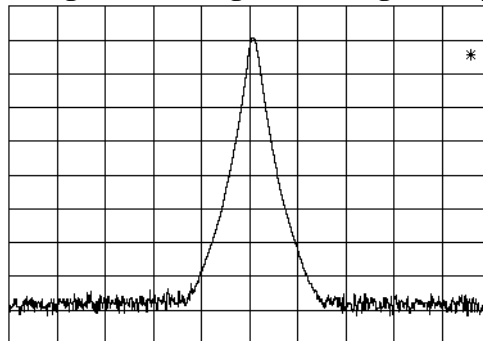
Measuring a Complex/Unknown Signal

NOTE   The steps below help to determine the signal analyzer settings when using time gating. The steps apply to the time gating approaches using gated LO and gated video.

This example shows you how to use time gating to measure a very specific signal. Most signals requiring time gating are fairly complex and in some cases extra steps may be required to perform a measurement.

Change step 1 or add additional step to include using Gate View in the analyzer vs. the o'scope to look at the signal in time domain.

   Step 1. Determine how your signal under test appears in the time domain and how it is synchronized

to the trigger signal.

You need to do this to position the time gate by setting the delay relative to the trigger signal. To set the delay, you need to know the timing relationship between the trigger and the signal under test. Unless you already have a good idea of how the two signals look in the time domain, you can examine the signals with an oscilloscope to determine the following parameters:

- Trigger type (edge or level triggering)

- Pulse repetition interval (PRI), which is the length of time between trigger events (the trigger period).

- Pulse width, or τ

- Signal delay (SD), which is the length of time occurring between the trigger event and when the signal is present and stable. If your trigger occurs at the same time as the signal, signal delay will be zero.

Figure 15.   Time-domain Parameters
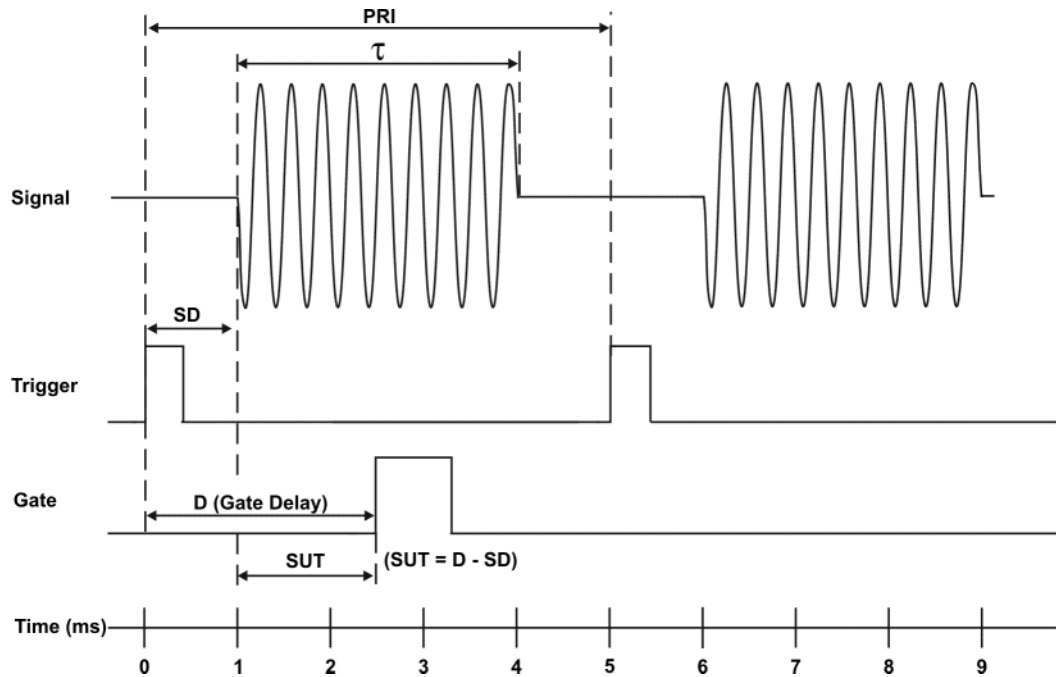
In Figure 15., the parameters are:

- Pulse repetition interval (PRI) is 5 ms.

- Pulse width (τ) is 3 ms.

- Signal delay (SD) is 1 ms for positive edge trigger (0.6 ms for negative edge trigger).

- Gate delay (D) is 2.5 ms.

- Setup time (SUT) is 1.5 ms.

Step 2. Set the signal analyzer sweep time:

Gated LO: Sweep time does not affect the results of gated LO unless the sweep time is set too fast. In the event the sweep time is set too fast, `Meas Uncal` appears on the screen and the sweep time will need to be increased.

Gated Video: Sweep time does affect the results from gated video. The sweep time must be set accordingly for correct time gating results. The recommended sweep time is at least the number of *sweep points – 1* multiplied by the *PRI (pulse repetition interval)*. Measurements can be made with sweep times as fast as (sweep points–1)*(PRI–τ).

Step 3. Locate the signal under test on the display of the signal analyzer. Set the center frequency and span to view the signal characteristics that you are interested in measuring. Although the analyzer is not yet configured for correct gated measurements, you will want to determine the approximate frequency and span in which to display the signal of interest. If the signal is erratic or intermittent, you may want to hold the maximum value of the signal with **Max Hold** (located under the **Trace/Detector** menu) to determine the frequency of peak energy.

To optimize measurement speed in the Gated LO case, set the span narrow enough so that the display will still show the signal characteristics you want to measure. For example, if you wanted to look for spurious signals within a 200 kHz frequency range, you might set the frequency span to just over 200 kHz.

Step 4. Determine the setup time and signal delay to set up the gate signal. Turn on the gate and adjust the gate parameters including gate delay and gate length as shown below.

Generally, the gate should be positioned over a part of the signal that is stable, not over a pulse edge or other transition that might disturb the spectrum. Starting the gate at the center of the pulse gives a setup time of about half the pulse width. Setup time describes the length of time during which that signal is present and stable before the gate comes on. The setup time (SUT) must be long enough for the RBW filters to settle following the burst-on transients. Signal delay (SD) is the length of time after the trigger, but before the signal of interest occurs and becomes stable. If the trigger occurs simultaneously with the signal of interest, SD is equal to zero, and SUT is equal to the gate delay. Otherwise, SUT is equal to the gate delay minus SD. See Figure 16.

Figure 16.   Positioning the Gate
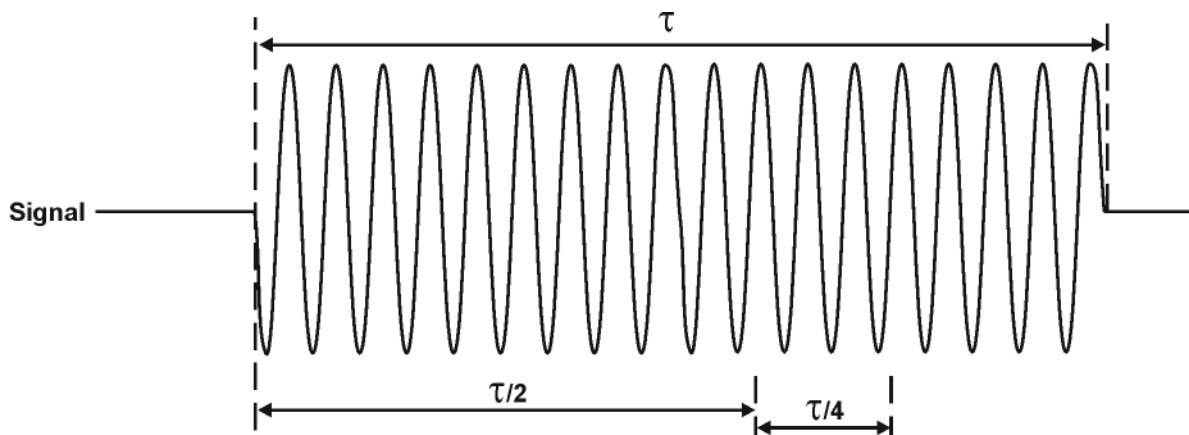
There is flexibility in positioning the gate, but some positions offer a wider choice of resolution bandwidths. A good rule of thumb is to position the gate from 20 % to 90 % of the burst width. Doing so provides a reasonable compromise between setup time and gate length.

Figure 17.   Best Position for Gate
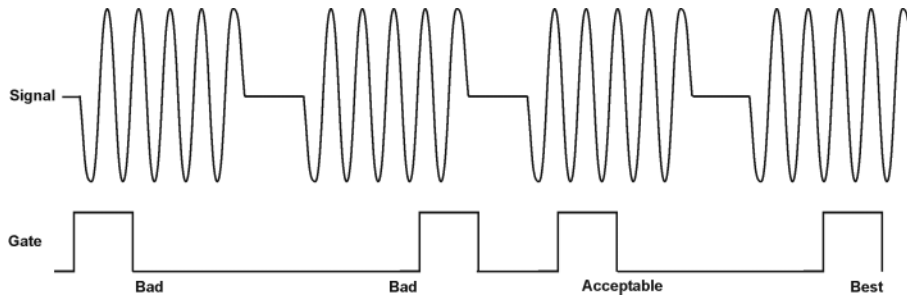
As a general rule, you will obtain the best measurement results if you position the gate relatively late within the signal of interest, but without extending the gate over the trailing pulse edge or signal transition. Doing so maximizes setup time and provides the resolution bandwidth filters of the signal analyzer the most time to settle before a gated measurement is made. "Relatively late," in this case, means allowing a setup time of at least 3.84/resolution bandwidth (see step 5 for RBW calculations).

As an example, if you want to use a 1 kHz resolution bandwidth for measurements, you will need to allow a setup time of at least 3.84 ms.

Note that the signal need not be an RF pulse. It could be simply a particular period of modulation in a signal that is continuously operating at full power, or it could even be during the off time between pulses. Depending on your specific application, adjust the gate position to allow for progressively longer setup times (ensuring that the gate is not left on over another signal change such as a pulse edge or transient), and select the gate delay and length that offer the best representation of the signal characteristics of interest on the display.

If you were measuring the spectrum occurring between pulses, you should use the same (or longer) setup time after the pulse goes away, but before the gate goes on. This lets the resolution bandwidth filters fully discharge the large pulse before the measurement is made on the low-level interpulse signal.

Figure 18.   Setup Time for Interpulse Measurement
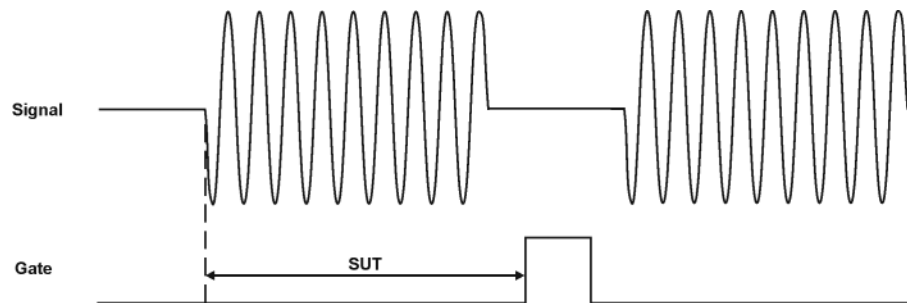
Step 5. The resolution bandwidth will need to be adjusted for gated LO and gated video. The video bandwidth will only need to be adjusted for gated video.

Resolution Bandwidth:

The resolution bandwidth you can choose is determined by the gate position, so you can trade off longer setup times for narrower resolution bandwidths. This trade-off is due to the time required for the resolution-bandwidth filters to fully charge before the gate comes on. Setup time, as mentioned, is the length of time that the signal is present and stable before the gate

comes on.

Figure 19.   Resolution Bandwidth Filter Charge-Up Effects
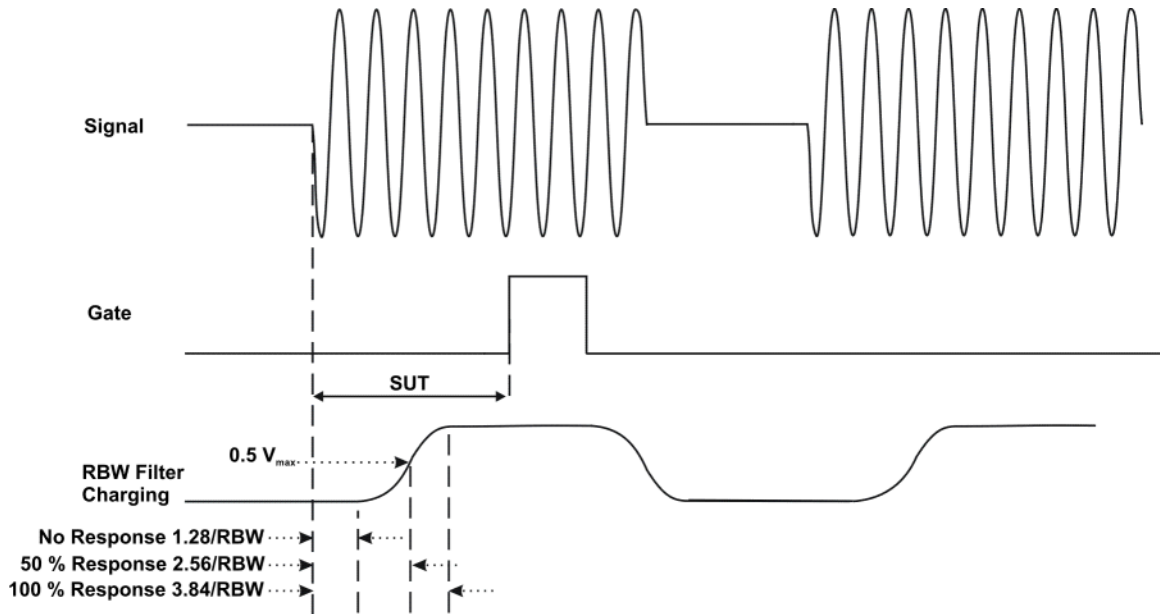
Because the resolution-bandwidth filters are band-limited devices, they require a finite amount of time to react to changing conditions. Specifically, the filters take time to charge fully after the analyzer is exposed to a pulsed signal.

Because setup time should be greater than filter charge times, be sure that:

$$SUT > \frac{3.84}{RBW}$$

where SUT is the same as the gate delay in this example. In this example with SUT equal to 1.5 ms, RBW is greater than 2.56 kHz; that is, RBW is greater than 1333 Hz. The resolution bandwidth should be set to the next larger value, 2.7 kHz.

Video Bandwidth:

For gated LO measurements the VBW filter acts as a track-and-hold between sweep times. With this behavior, the VBW does not need to resettle on each restart of the sweep.

Step 6. Adjust span as necessary, and perform your measurement.

The analyzer is set up to perform accurate measurements. Freeze the trace data by activating single sweep, or by placing your active trace in view mode. Use the markers to measure the signal parameters you chose in step 1. If necessary, adjust span, but do not decrease resolution bandwidth, video bandwidth, or sweep time.

"Quick Rules" for Making Time-Gated Measurements

This section summarizes the rules described in the previous sections.

Table 1. Determining Signal Analyzer Settings for Viewing a Pulsed RF Signal

Signal Analyzer Function	Signal Analyzer Setting	Comments
Sweep Time (gated video only)	Set the sweep time to be equal to or greater than (number of sweep points - 1) × pulse repetition interval (PRI):	Because the gate must be on at least once per trace point, the sweep time should be set such that the sweep time for each trace point is greater than or equal to the pulse repetition interval.
Gate Delay	The gate delay is equal to the signal delay plus one-fourth the pulse width: Gate Delay = Signal Delay + $\tau/5$	The gate delay must be set so that the gating captures the pulse. If the gate delay is too short or too long, the gating can miss the pulse or include resolution bandwidth transient responses.
Gate Length	The gate length minimum is equal to one-fourth the pulse width (maximum about one-half): Gate Length = 0.7 x $\tau/4$	If the gate length is too long, the signal display can include transients caused by the signal analyzer filters. The recommendation for gate placement can be between 20 % to 90 % of the pulse width.
Resolution Bandwidth	Set the resolution bandwidth: RBW > 19.5/τ	The resolution bandwidth must be wide enough so that the charging time for the resolution bandwidth filters is less than the pulse width of the signal.

Figure 20.   Gate Positioning Parameters
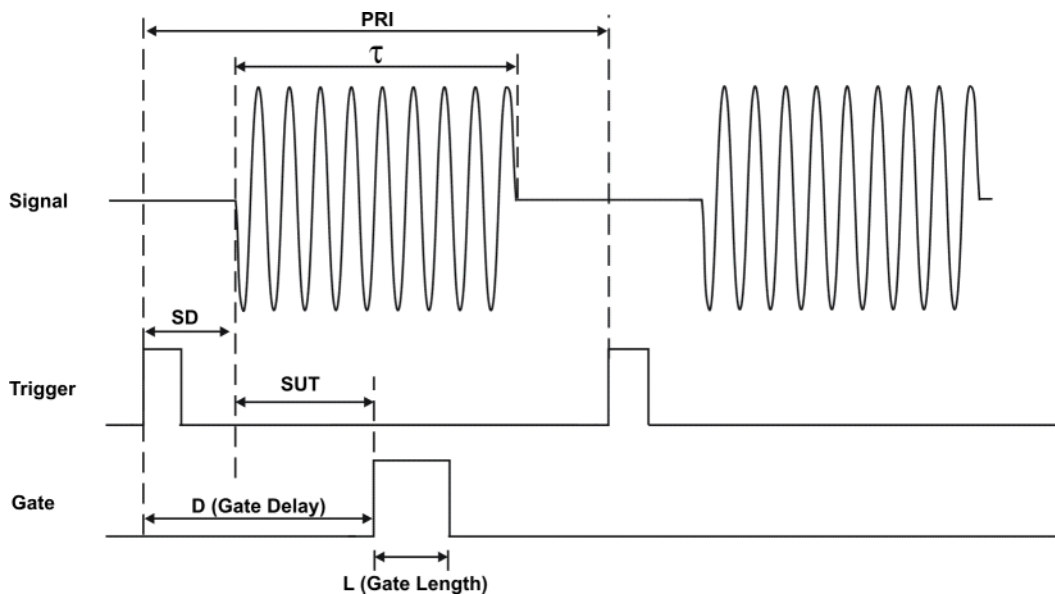
Most control settings are determined by two key parameters of the signal under test: the pulse repetition interval (PRI) and the pulse width (τ). If you know these parameters, you can begin by picking some standard settings. Table 2. summarizes the parameters for a signal whose trigger event occurs at the same time as the beginning of the pulse (in other words, SD is 0). If your signal has a non-zero delay, just add it to the recommended gate delay.

Table 2. Suggested Initial Settings for Known Pulse Width (τ) and Zero Signal Delay

Pulse width (τ)	Gate Delay (SD + τ/5)	Resolution Bandwidth (>19.5/τ)	Gate Length (0.7 x τ/4)
4 µs	0.8 µs	4.875 MHz	0.7 µs
10 µs	2 µs	1.95 MHz	1.753 µs
50 µs	10 µs	390 kHz	8.75 µs
63.5 µs	12.7 µs	307 kHz	11.11 µs
100 µs	20 µs	195 kHz	17.5 µs
500 µs	100 µs	39 kHz	87.5 µs
1 ms	200 µs	19.5 kHz	0.175 µs
5 ms	1 ms	3.9 kHz	0.875 ms
10 ms	2 ms	1.95 kHz	1.75 ms
16.6 ms	3.32 ms	1.175 kHz	2.905 ms
33 ms	6.6 ms	591 Hz	5.775 ms
50 ms	10 ms	390 Hz	8.75 ms
100 ms	20 ms	195 Hz	17.5 ms
≥130 ms	26 ms	151 Hz	22.75 ms

Table 3. If You Have a Problem with the Time-Gated Measurement

Symptom	Possible Causes	Suggested Solution
Erratic analyzer trace with dropouts that are not removed by increasing analyzer sweep time; oscilloscope view of gate output signal jumps erratically in time domain.	Gate Delay may be greater than trigger repetition interval.	Reduce Gate Delay until it is less than trigger interval. Check **Gate View** to make sure the gate delay is timed properly.
Gate does not trigger.	1) Gate trigger voltage may be wrong. 2) Gate may not be activated. 3) **Gate Source** selection may be wrong.	With external gate trigger: ensure that the trigger threshold is set near the midpoint of the waveform (view the waveform on and oscilloscope using high input impedance, not 50 Ω). With RF Burst Gate Source: ensure that the start and stop frequencies are within 10 MHz of the center frequency of the carrier. Check to see if other connections to trigger signal may be reducing voltage. If using an oscilloscope, check that all inputs are high impedance, not 50 Ω.
Display spectrum does not change when the gate is turned on.	Insufficient setup time.	Increase setup time for the current resolution bandwidth, or increase resolution bandwidth.
Displayed spectrum too low in amplitude.	Resolution bandwidth or video bandwidth filters not charging fully.	Widen resolution bandwidth or video bandwidth, or both.

## Using the Edge Mode or Level Mode for Triggering

Depending on the trigger signal that you are working with, you can trigger the gate in one of two separate modes: edge or level. This gate-trigger function is separate from the normal external trigger capability of the signal analyzer, which initiates a sweep of a measurement trace based on an external signal.

Edge Mode

Edge mode lets you position the gate relative to either the rising or falling edge of a trigger signal. The left diagram of Figure 21. shows triggering on the positive edge of the trigger signal while the right diagram shows negative edge triggering.

Example of key presses to initiate positive edge triggering:
Press **Sweep**, **Gate**, **More**, **Polarity** (Pos).

Figure 21.   Using Positive or Negative Edge Triggering
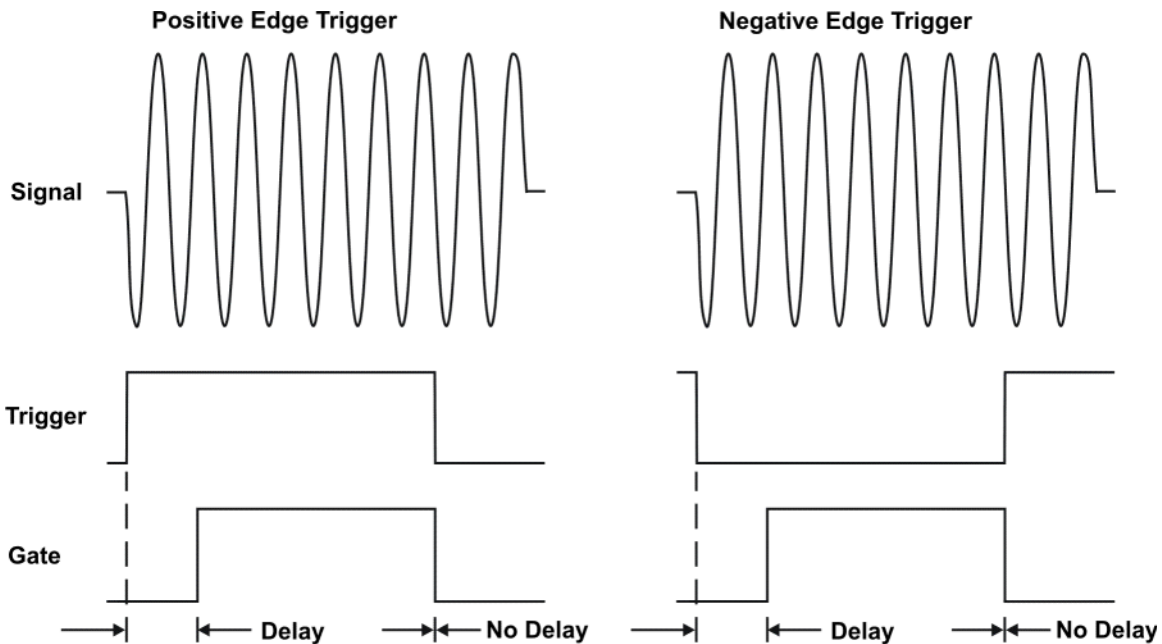
Level Mode

In level gate-control mode, an external trigger signal opens and closes the gate. Either the TTL high level or TTL low level opens the gate, depending on the setting of **Trig Slope**. Gate delay affects the start of the gate but not the end. Gate length is applicable when using level mode triggering. Level mode is useful when your trigger signal occurs at exactly the same time as does the portion of the signal you want to measure.

Noise Measurements Using Time Gating

Time gating can be used to measure many types of signals. Noise and noise-like signals are often a special case in spectrum analysis. With the history of gated measurements, these signals are especially noteworthy.

The average detector is the best detector to use for measuring noise-like signals because it uses all the available noise power all the time in its measurement. The sample detector is also a good choice because it, too, is free from the peak biases of the peak detector, normal and negative peak detectors.

When using the average or sample detector, noise density measurements using the noise marker or band/interval density marker can be made without any consideration of the use of gating--gated measurements work just as well as non-gated measurements. Thus, the average detector is recommended for noise density measurements.

Older analyzers only had the gated video version of gating available, and these only worked with the peak detector, so the rest of this section will discuss the trade-offs associated with trying to replicate these measurements with an X-Series analyzer.

Unlike older analyzers, X-Series analyzers can make competent measurements of noise density using the noise marker with all detectors, not just those that are ideal for noise measurements. Thus, X-Series analyzers can make noise density measurements with peak detection, compensating for the extent to which peak detection increases the average response of the analyzer to noise. When comparing a gated video measurement using the noise marker between an X-Series and an older analyzer where both use the peak detector, the X-Series answer will be approximately correct, while the older analyzer will need a correction factor. That correction factor is discussed in Agilent Technologies Application Note 1303, Spectrum Analyzer Measurements and Noise, in the section on Peak-detected Noise and TDMA ACP Measurements.

When making measurements of Band/Interval Power or Band/Interval Density, the analyzer does not make compensations for peak detection. For best measurements with these marker functions, average or sample detection should be used.